MOS Transistors Models

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The MOS transistor – Levels of Abstraction -

Model Equations

If $V_{GS} < 0$

$I_{DS} = 0$

If $V_{DS} > V_{GS} - V_{TO}$

$I_{DS} = \left( \frac{W}{L} \right) \frac{UO}{2} \frac{e_0 e_r}{TOX} (V_{GS} - V_T)^2$

If $V_{DS} < V_{GS} - V_{TO}$

$I_{DS} = \left( \frac{W}{L} \right) UO \frac{e_0 e_r}{TOX} \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$

$V_T = V_{TO} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$

MATHEMATICAL

PHYSICAL

Model Current-Voltage Characteristics

55nm SST Flash Cell

Current – Voltage Characteristics

SEM photograph

Layout

Symbol

NMOS  PMOS
What is a model?

1. An intuitive and conceptual abstraction of a complex physical process

2. A mathematical abstraction of a complex physical process that is capable of predicting experimental observations.
What is a MODEL?

1. An intuitive and conceptual abstraction of a complex physical process

2. A mathematical abstraction of a complex physical process that is capable of predicting experimental observations.
MOS fluidic analogy: a conceptual model (I)  

From Mead and Conway

MOS Capacitor

MOS Transistor Varia Bias

MOS Transistor
NMOS as a switch/resistor: a conceptual model (II)

[Diagram showing the NMOS switch in both off and on states, with explanations of electron movement and voltage levels.]
PMOS as a switch/resistor: a conceptual model (III)
What are the physical values for 0 and 1 chip/logic voltages (blue line)
MOS switch model relation to I-V characteristics (I)

With digital input on gate the device is either ON or OFF

180nm technology
MOS switch model relation to I-V characteristics (II)

With digital input on gate the device is either ON or OFF

Approximate ON with the blue line

\[ R_{ON} \approx \frac{3.3 \text{ V}}{0.55 \text{ mA}} = 6K \]
What is a MODEL?

1. An intuitive and conceptual abstraction of a complex physical process

2. A mathematical abstraction of a complex physical process that is capable of predicting experimental observations.
Conduction – ohmic- vs saturation

Device operation characterized by the form of the current as a function of the bias voltage between the DRAIN and the source terminals (Vds)

Conduction (also known as Ohmic)

Saturation
Above threshold vs sub-threshold behaviour

Device operation characterized by the form of the current as a function of the bias voltage between the gate and the source terminals (Vgs)
MOS transistor mathematical model
Mathematical model –above threshold-

If \( V_{GS} < 0 \)
\( I_{DS} = 0 \)

If \( V_{DS} > V_{GS} - V_{TO} \)
\( I_{DS} = \left( \frac{W}{L} \right) \left( \frac{UO}{2} \right) \frac{\varepsilon_0 \varepsilon_r}{TOX} \left( V_{GS} - V_T \right)^2 \)

If \( V_{DS} < V_{GS} - V_{TO} \)
\( I_{DS} = \left( \frac{W}{L} \right) UO \frac{\varepsilon_0 \varepsilon_r}{TOX} \left( V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \)

\( V_T = V_{TO} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \)

\( \varepsilon_0 = 8.85 \times 10^{-12} \text{ F/m} \) is the absolute permittivity
\( \varepsilon_r = \) relative permittivity, equal to 3.9 in the case of SiO2 (no unit)

<table>
<thead>
<tr>
<th>MOS Model 1 parameters</th>
<th>Typical Value 0.12( \mu )m</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{TO} )</td>
<td>Theshold voltage</td>
<td>0.4V</td>
<td>-0.4V</td>
</tr>
<tr>
<td>( U0 )</td>
<td>Carrier mobility</td>
<td>0.06m(^2)/V-s</td>
<td>0.02m(^2)/V-s</td>
</tr>
<tr>
<td>TOX</td>
<td>Gate oxide thickness</td>
<td>2nm</td>
<td>2nm</td>
</tr>
<tr>
<td>PHI</td>
<td>Surface potential at strong inversion</td>
<td>0.3V</td>
<td>0.3V</td>
</tr>
<tr>
<td>GAMMA</td>
<td>Bulk threshold parameter</td>
<td>0.4 V(^{0.5})</td>
<td>0.4 V(^{0.5})</td>
</tr>
<tr>
<td>W</td>
<td>MOS channel width</td>
<td>1( \mu )m</td>
<td>1( \mu )m</td>
</tr>
<tr>
<td>L</td>
<td>MOS channel length</td>
<td>0.12( \mu )m</td>
<td>0.12( \mu )m</td>
</tr>
</tbody>
</table>

Model parameters
Above threshold vs sub-threshold behaviour

Device operation characterized by the form of the current as a function of the bias voltage between the gate and the source terminals (Vgs)
Mathematical model – subthreshold –

\[ I_D \equiv I_{DS} = S I_n 0 \exp\left(\frac{\kappa n V_{GB}}{V_t}\right) \left[ \exp\left(\frac{-V_{SB}}{V_t}\right) - \exp\left(\frac{-V_{DB}}{V_t}\right) \right] \]

\[ I_D \equiv I_{SD} = S I_p 0 \exp\left(\frac{-\kappa p V_{GB}}{V_t}\right) \left[ \exp\left(\frac{V_{SB}}{V_t}\right) - \exp\left(\frac{V_{DB}}{V_t}\right) \right] \]

\[ V_t \equiv \frac{kT}{q} \quad \kappa \equiv \frac{1}{\eta} = \frac{C_{ox}}{C_{ox} + C_{dep}} \quad S \equiv \frac{W}{L} \]

Parameters:

\[ I_{p0} = 0.5 \times 10^{-18} \text{ A} \]

\[ I_{n0} = 0.9 \times 10^{-18} \text{ A} \]

\[ \kappa = 0.7 \]

\[ V_t = 0.26 \text{ Volts} \]
Operating current for an NMOS

- Operates on one of two curves
  - on
    - Looks like a current source initially (high $V_{ds}$)
    - Looks like a resistor later (low $V_{ds}$)
  - off
    - Open circuit always
Operating current for a PMOS

- Same behavior as NMOS
  - Open circuit when off
  - Current source or resistor when on
Computer Aided Design Tools

MICROWIND Tool Design Flow

Contact:
Sales: sales@microwind.net
Support: support@microwind.net

SPICE Simulator (3rd Party)

Schematic Modeling
Analog & digital Library models

Digital Simulation
Verilog Extraction
SPICE Extraction

DSCH 3

Verilog File

ModelSim / other

Synthesis
Functional Simulation
Floorplanning
Place & Route
Programming File .bit or .jed

FPGA Tools

Verilog Compiler

Constraints

Technology rule files

Analysis
DRC, ERC
Delay Analyzer
Crosstalk Analyzer
2D Cross section
3D Analyzer

Place & Route

Layout Extraction

ProTHUMB
Advance post layout simulator

Layout Conversion

SPICE, CIF

Layout Editor

Verilog Compiler

Verilog File

nanolambda

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FPGA Tools

IO Cards
Traffic Light Controller, Key Pad, Display (LCD, 7 segs)

FPGA / CPLD Boards

MICROWIND Tool

3rd Party Tools

LTSpice
WindSpice

http://www.microwind.net