Lecture 8
Local and Global Interconnects
Modeling Interconnects – capacitance of a single wire-

Figure 5-18: One conductor above a ground plane

\[
C = C_s + 2C_f = \varepsilon_0\varepsilon_r \left( 1.13 \frac{W}{e} + 1.44 \left( \frac{W}{e} \right)^{0.11} + 1.46 \left( \frac{t}{e} \right)^{0.42} \right)
\]  

(5-2)

- **C** = total capacitance per meter (Farad/m)
- **Cs** = surface capacitance (Farad/meter)
- **Cf** = fringing capacitance (Farad/m)
- \(\varepsilon_0\) = 8.85 \(\times\) 10\(^{-12}\) Farad/m
- \(\varepsilon_r\) = 3.9 for SiO\(_2\)
- **w** = conductor width (m)
- **t** = conductor thickness (m)
- **e** = dielectric thickness (m)
wires everywhere!
Modeling Interconnects – capacitance of two wires.

Figure 5-20: Two conductors above a ground plane

\[ C = C_s + C_f = \varepsilon_0 \varepsilon_r (1.10 \frac{W}{e} + 0.79 (\frac{W}{e})^{0.1} + 0.46 (\frac{t}{e})^{0.17} (1 - 0.87 e^{(-\frac{d}{e})} )) \]  \hspace{1cm} (5-3)

\[ C_{12} = \varepsilon_0 \varepsilon_{r,low} \left( \frac{t}{d} + 1.2 (\frac{d}{e})^{0.1} \left( \frac{d}{e} + 1.15 \right)^{-2.22} + 0.253 \ln(1 + 7.17 \frac{W}{d}) \left( \frac{d}{e} + 0.54 \right)^{-0.64} \right) \]  \hspace{1cm} (5-4)

C = conductor capacitance to ground per meter (Farad/m)
Cs = surface capacitance (Farad/meter)
Modeling Interconnects – layout capacitance example –

Figure 5-21: Example of interconnects routed in metal 1, 2 and 3

- **High K dielectric**
  - Conductor above substrate (Y0-Y0)
  - $C = C_1 = 70 \text{fF/mm}$

- **High K dielectric**
  - One conductor, one plane (Y1-Y1)
  - $C = C_1 = 120 \text{fF/mm}$

- **High K dielectric**
  - One conductor, two planes (Y2-Y2)
  - $C = C_1 + C_{1b} = 150 \text{fF/mm}$

- **Two conductors, one plane (Y3-Y3)**
  - $C = C_1 = 90 \text{fF/mm}$
  - $C_{12} = 50 \text{fF/mm}$

- **Low K**
  - $C_1$
Interconnect resistance

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistivity Type</th>
<th>Component</th>
<th>Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\rho_{Ag}$</td>
<td>Gold resistivity</td>
<td>Bonding between chip and package</td>
<td>$2.20 \times 10^{-8} \Omega \cdot cm$</td>
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<tr>
<td>$\rho_{tungsten}$</td>
<td>Tungsten resistivity</td>
<td>Contacts</td>
<td>$5.30 \times 10^{-8} \Omega \cdot cm$</td>
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<tr>
<td>$\rho_{N^+}$</td>
<td>Highly doped silicon resistivity</td>
<td>N+ diffusions</td>
<td>$0.25 \Omega \cdot cm$</td>
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<tr>
<td>$\rho_{Nwell}$</td>
<td>Lightly doped silicon resistivity</td>
<td>N well</td>
<td>$50 \Omega \cdot cm$</td>
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<tr>
<td>$\rho_{Si}$</td>
<td>Intrinsic silicon resistivity</td>
<td>Substrate</td>
<td>$2.5 \times 10^5 \Omega \cdot cm$</td>
</tr>
</tbody>
</table>

Table 5-3: Resistivity of several materials used in CMOS circuits

![Diagram of a conductor](image)

**Figure 5-26: Resistance of a conductor**

$$R = \rho \frac{l}{w \cdot t} \quad (\text{Eqn. 5-5})$$

where

- $R$ = serial resistance (ohm)
- $\rho$ = resistivity (ohm.m)
- $w$ = conductor width (m)
- $t$ = conductor thickness (m)
- $l$ = conductor length (m)
- $d$ = conductor distance (m)
Estimating resistance of a wire – measuring squares –

\[ 0.05 \times 10 = 0.5 \Omega \]
Interconnect resistance scaling

0.35μm: Alu 35mΩ
0.25μm: Alu 75mΩ
0.12μm: Copper 50mΩ
90nm: Copper 60mΩ

Interconnect resistance/μm

Technological generation
Via resistance

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.7μm</th>
<th>0.12μm</th>
<th>90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact resistance</td>
<td>0.5 Ω</td>
<td>15 Ω</td>
<td>20 Ω</td>
</tr>
<tr>
<td>Via</td>
<td>0.3 Ω</td>
<td>4 Ω</td>
<td>8 Ω</td>
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<tr>
<td>Upper via</td>
<td>-</td>
<td>1 Ω</td>
<td>3 Ω</td>
</tr>
</tbody>
</table>

![Via resistance diagram](image-url)
Modeling interconnects

Lumped parameter: (C)

Distributed: (R-C)
Simulation

(a) 10mm, metal 3, 0.35\textmu m technology
Modeling interconnects (II)

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Figure 5-43: Below 1mm, the C model is valid. Above 1mm, the RC model should be considered in 0.12 μm CMOS technology.
how about inductance?

\[ L = \frac{\mu_0}{2\pi} \ln \left( \frac{h}{d} \right) \]  
(Equ. 5-7)

with

- \( \mu_0 = 1.257 \times 10^6 \) H/m for most materials (Al, Cu, Si, SiO2 and Si3N4)
- \( d \) = wire diameter (m)
- \( h \) = height of the wire vs. ground (m)
transistor and interconnect models

A Pair of Inverters

RC-Network for Timing Analysis

RC-Network for Timing Analysis (trimmed)