520/530/580.495 Microfabrication Laboratory

Laboratory Assignment

Instrumentation and Measurements

Mask Design Using LEDIT

This week we will learn how to do the physical layout for designing masks using the program LEDIT.

LAB OBJECTIVES

1. To get familiar with the physical layout editor LEDIT for designing masks

I. PRELAB WORK

1. Browse the web page for the class project done a decade ago in our lab! (click on the Fall 2004 link in the archives section of our website). Read the final reporrt by T. Edwards (http://www.ece.jhu.edu/~andreou/495/Archives/1994/TE94Report/sensor.html)

2. Download the zip archive (Lab1bFiles.zip) with the necessary files for this laboratory assignment from the course web site.

http://www.ece.jhu.edu/~andreou/495/LabWork/Lab1bFiles.zip

3. Get the LEDIT 11 User Guide from the installation directory of LEDIT and print out the Quick Reference Guide.

II. LAB WORK

1. Login in one of the Windows machine in the Microfab Lab (non-clean room area).
2. Open the LEDIT 11 User Guide in Acrobat and read Section 1 pages 28 to 227. While reading through, practice the various commands and make sure that you are familiar with the program. While at this, you may want to printout the LEDIT Quick Reference Guide to have it handy. (Do not spend more than three hours on this question!
3. Start the program and load the file *PXMask.tdb*. You will see the various structures that make up the MEMS pressure sensor because they are coded by different colors and patterns. The diffusion mask patterns are green, the metallization mask patterns are blue, the contact cuts are black and the membrane etch mask is coded by purple grid pattern. The design is done hierarchically and you can navigate through the individual cells. If you make changes in a leaf cell, these changes will manifest themselves to all instances of the leaf cell. As our lab facilities are limited the number of mask steps are also limited. A typical CMOS process has a minimum of nine mask layers and more advance processes will have eleven or twelve. The design is done on a grid and

the size of the basic grid spacing is one lambda. This is a parameter that depends on the process. For example, state of the art CMOS processes today have a lambda of 90nm!

4. Calculate the dimensions of the basic structures on the mask. Get a hardcopy of the design by printing it and indicate on it these dimensions. What do you think lambda is for our process?
5. Congratulations! You have learned how do create your own mask design.

III. Postlab Work:

1. Check out MOSIS (Metal Oxide Semiconductor Implementation Service), a silicon foundry that provides services for state of the art IC processes. What is the state of the art fabrication process offered by the foundry today? How many metal layers and how many polysilicon layers are offered in this process?
2. Ask the Lab Assistants to show you the mask set for this project.
3. Do the design of the masks for your project in LEDIT. Pay attention to the alignment marks. Make sure that you do not modify the locations of the alignment marks in the different layers (extra credit for undergraduate students, REQUIRED for graduate students). The mask design is due the last day of classes.

BIBLIOGRAPHY

1. Download from the CAD Lab and Resources section of the course website. Alternatively, the LEDIT user guides and quick reference guides can be accessed through “START/Programs/Tanner EDA”, or in the installation directories for the respective programs. In the ECE computers these programs are installed in:

- C:\Program Files\Tanner EDA\L-Edit 11.0

Lab procedure prepared by A.G. Andreou, Fall 2004, Fall 2015.