520.487
Introduction to MEMS

Integrated Circuits Fabrication
and
Very Large Scale Integration

MEMS Foundry Technologies
Integrated Circuit Fabrication

Mask set

Film formation

Lithography

Etching

Impurity doping

Wafer out
VLSI and MOSIS (Metal Oxide Semiconductor Implementation System)

- AMI 0.35, 0.5 and 1.5 micron CMOS
- TSMC 0.35, 0.25 and 0.18 micron CMOS
- IBM SiGe 0.25, 0.18 micron BiCMOS
- Peregrine 0.5 micron SOS CMOS

http://www.mosis.org/

Key idea: Use a number of different manufacturers to contribute manufacturing capacity to multiuser projects.

520.216, 520.492 will teach you how to analyze and design analog and digital integrated circuits.
Bulk CMOS Technology (I)

n-well

p-substrate

Polysilicon 1

p^{++}

n^{++}
Bulk CMOS Technology (II)

polysilicon 2

contact

metal 1
Bulk CMOS Technology (III)

vias

metal 2

metal 3
Bulk CMOS Technology (IV)

P-BASE option
Basic CMOS components

- Conductors
- Switches (MOS transistors)
- Capacitors (MOS capacitors)
- Inductors
- Resistors
MOS Transistor Fabrication Details (I)

(a) 

![Diagram of MOS transistor layers: Photoresist, Si₃N₄, SiO₂, p-Si <100>]

(b) 

![Diagram showing Boron field implant and Active device area]

(c) 

![Diagram depicting Boron channel implant, Field oxide, Self-aligned chanstop, Gate oxide]

(d) 

![Diagram illustrating Patterned polysilicon gate and p⁺]
MOS Transistor Fabrication Details (II)

(a) Arsenic implant

(b) Flowed P-glass

(c) Contact metallization

(d) Gate

Source

Drain

$\text{p-Si (100)}$

$L_G$

Active device area

Z
CMOS Inverter

(a)

(b)

(c)
DRAM Fabrication Details

(a) Row line
Access transistor
Storage capacitor
Column line

(b) Diffused column line
Window
Access transistor (polysilicon)
Polysilicon cell plate
Metal row line
Capacitor

(c) Transfer gate
Source
Inversion regions
Drain
Oxide

(d) Transfer gate
Storage gate

A.G. Andreou, 520.487 Summer 08
Metallization Details (PowerPC)
MicroElectroMechanical Systems (MEMS)

- MEMS
- MEMS before CMOS
  - Analog Devices i-MEMS
    Process mechanical structures before CMOS.
- MEMS after CMOS
  - Berkeley SiGe MEMS
    Process mechanical structures after CMOS being careful not to affect CMOS
- MEMS in CMOS
  - Post-processing Bulk CMOS (Fedder, Carnegie Mellon)
  - Post-processing SOI CMOS
MUMP
(MultiUser MEMS Process)

- PolyMUMP: 3 layer polysilicon surface micromachining
- SOIMUMP: 3 mask Silicon On Insulator bulk micromachining
- MetalMUMP: electroplated nickel process.
- ASIMPS: MEMS on CMOS using Jazz SiGe CMOS technology

Key idea: Use a series of functional layers combined with sacrificial layers to produced desired structures


This course will teach you how to design Microsystems (MEMS) in foundry technologies!
MUMPS Surface Micromachining

Patterned 1st polysilicon layer

Passivated substrate

Dimples patterned on PSG

Anchors patterned on 1st PSG layer

Patterned 2nd Polysilicon layer

Blanket 2nd PSG layer

Hub anchor

Patterned 3rd polysilicon layer

PSG removal

Bushing  Rotor  Hub  Ground  Stat

(a)
Spinning Gear
Lithographic, Galvanoformung, Abformung
LIGA Technology (I)

- Lithography
- Electroplating
- Molding
LIGA Process (II)

THICK 10um to 1mm MICROSTRUCTURES
MEMS with SOI-CMOS

• Build CMOS MEMS structures using stacked metal and oxide layers

• Release steps
  – Step 1 vertical etch down to sapphire substrate
  – Step 2 lateral sacrificial release layer etch to free MEMS
MEMS with SOI-CMOS examples

JHU Silicon on sapphire CMOS MEMS test chip