Manufacturing process and design rules
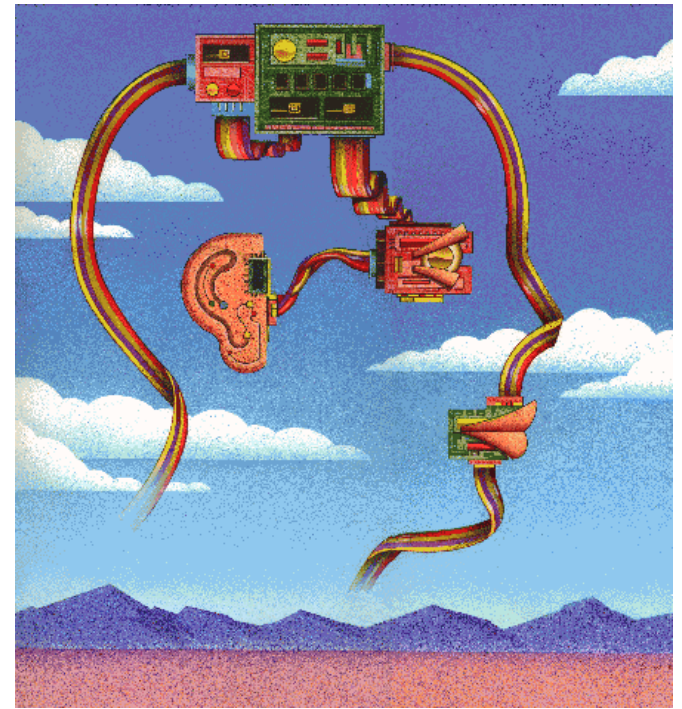

Andreas G. Andreou
Pedro Julian

Electrical and Computer Engineering
Johns Hopkins University

http://andreoulab.net

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1

Levels of Abstraction –the CMOS Inverter-

Out = NOT (In)

Out = ~ (In)

Equation

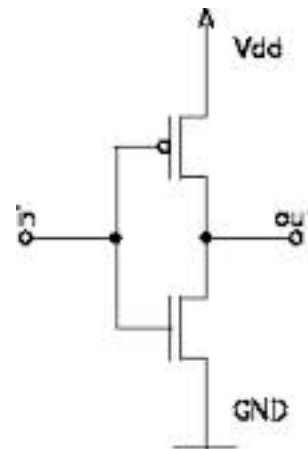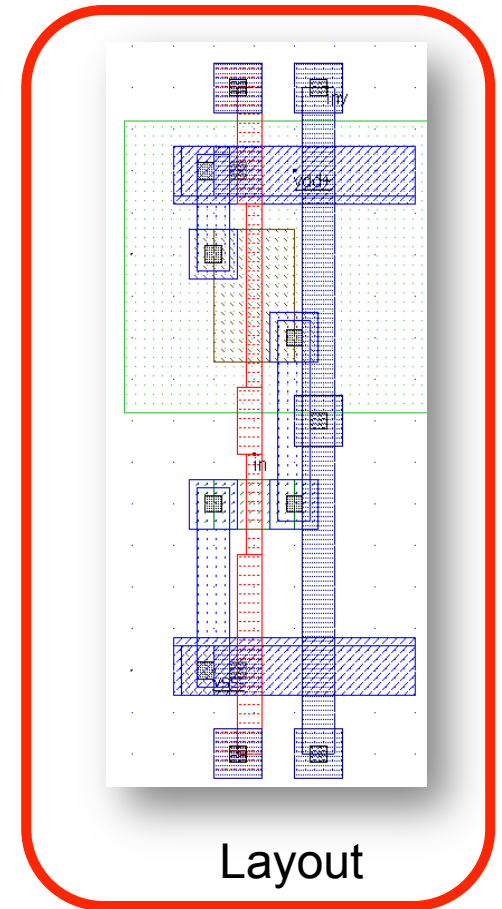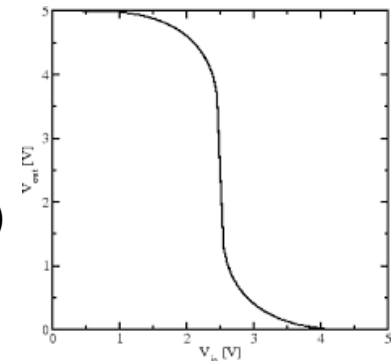| In	Out
0	1
1	0
X	X

Truth Table
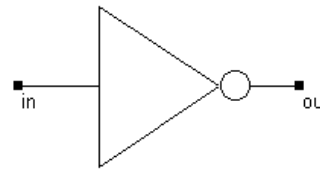
Symbol

Circuit

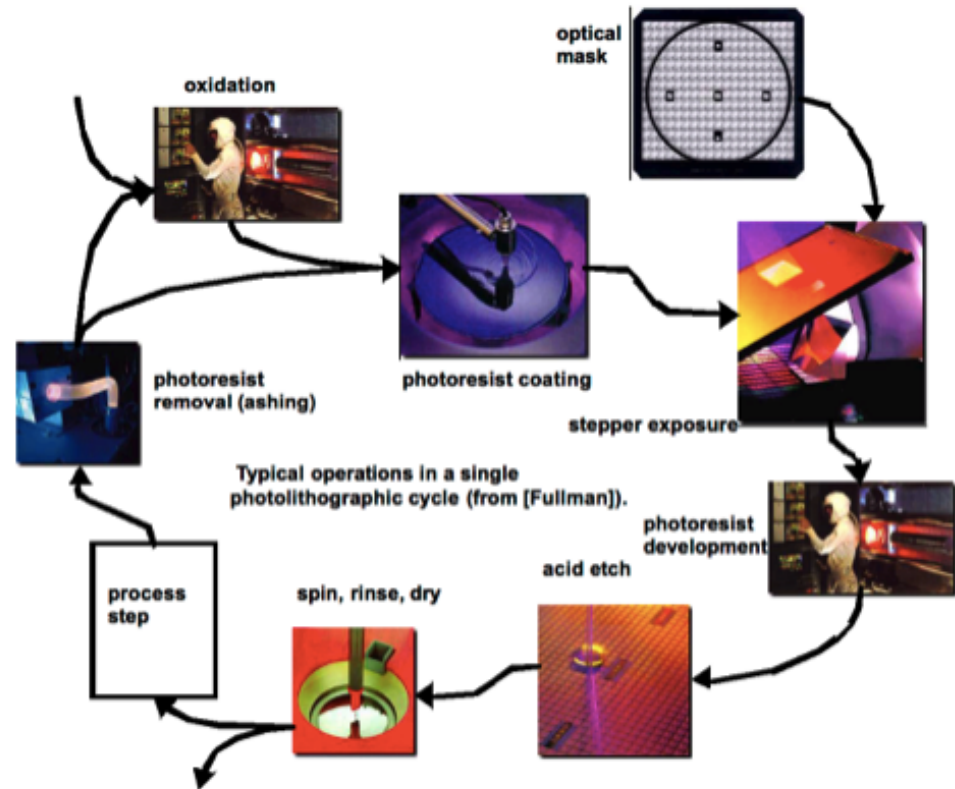Voltage Transfer
Characteristics (VTC)

Layout

LOGICAL | PHYSICAL

Introduction to VLSI Systems

2

CMOS Fabrication

Photolithography

CMOS Fabrication flow:

- Define active areas
  Etch and fill trenches
- Implant well regions
- Deposit and pattern polysilicon layer
- Implant source and drain regions and substrate contacts
- Create contact and via windows
  Deposit and pattern metal layers

Photolithography cycle labels:

oxidation

optical mask

photoresist coating

stepper exposure

photoresist removal (ashing)

Typical operations in a single photolithographic cycle (from [Fullman]).

photoresist development

process step

spin, rinse, dry

acid etch

Patterning of silicon dioxide

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

(d) After development and etching of resist, chemical or plasma etch of SiO_2

(e) After etching

(f) Final result after removal of resist

Designing an inverter

Fabrication Process (I)

(a) p-substrate

(b) SiO$_2$ / p-substrate

(c) Photoresist / SiO$_2$ / p-substrate

(d) Photoresist / SiO$_2$ / p-substrate

(e) Photoresist / SiO$_2$ / p-substrate

(f) SiO$_2$ / p-substrate

(g) SiO$_2$ / n-well / p-substrate

(h) n-well / p-substrate
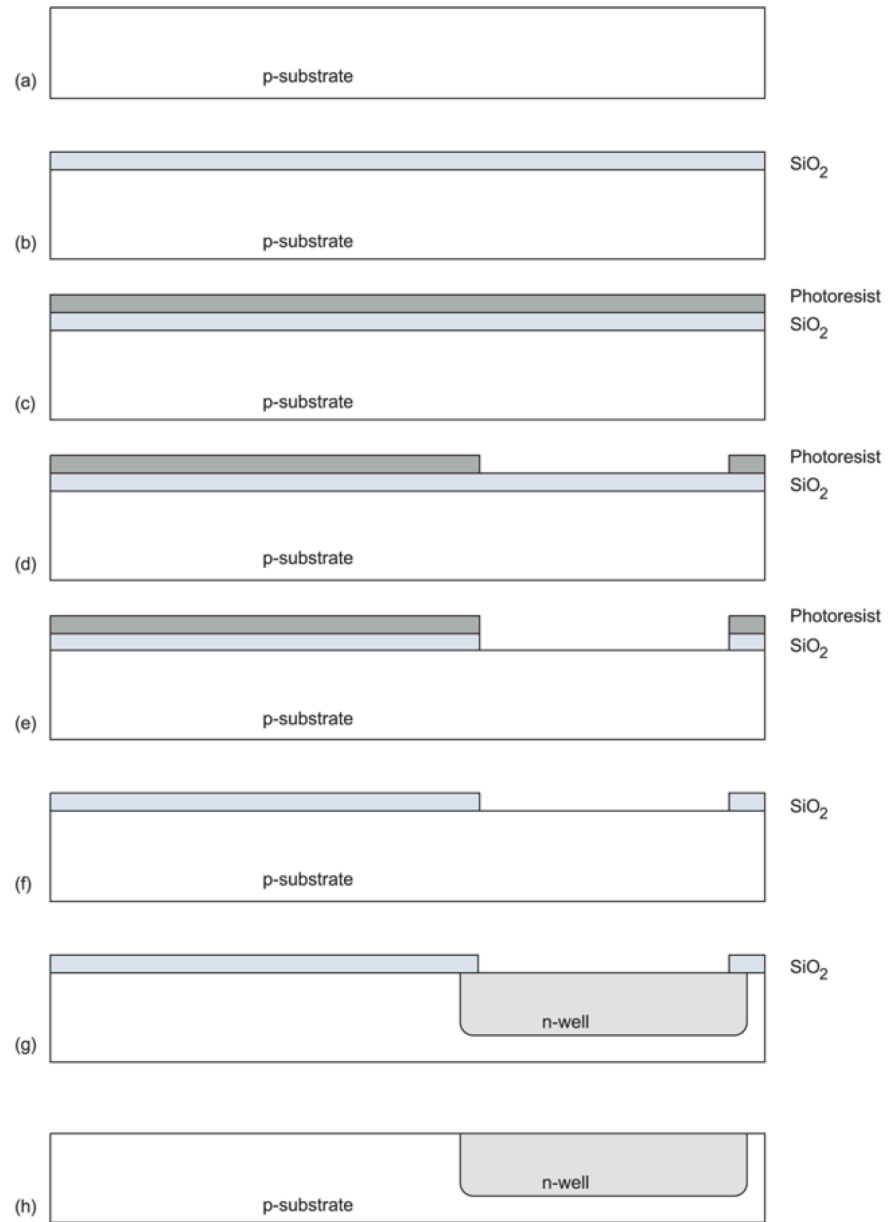
Fabrication Process (II)

Process cross-section
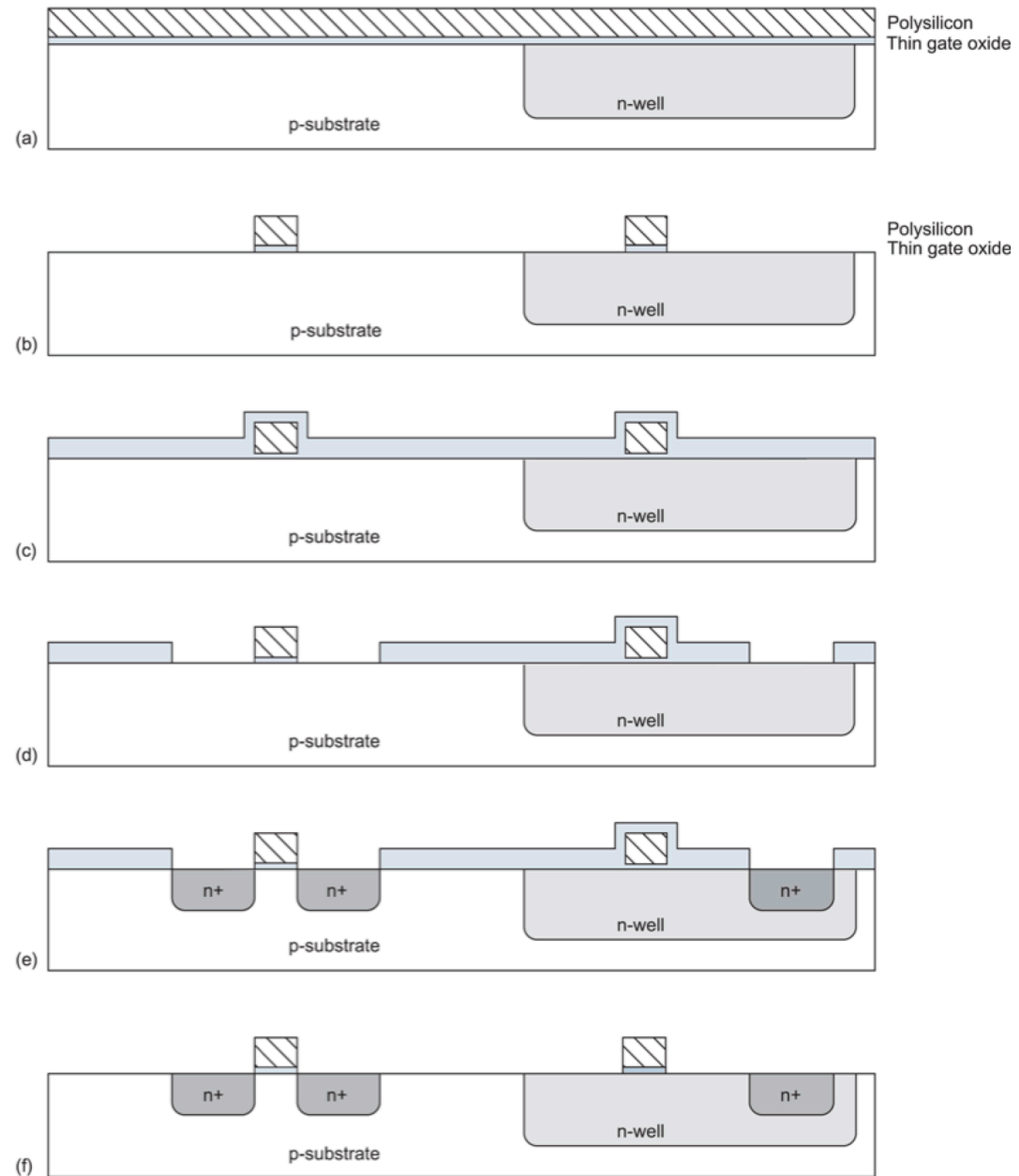
Design Rules

- The interface between the design engineer (you!) and the process engineer (the guys in the white space suits!)
- Guidelines for constructing masks (constraints)
- Dimensions:
    - Dimensionless (lambda parameter)
    - Absolute (nanometer)

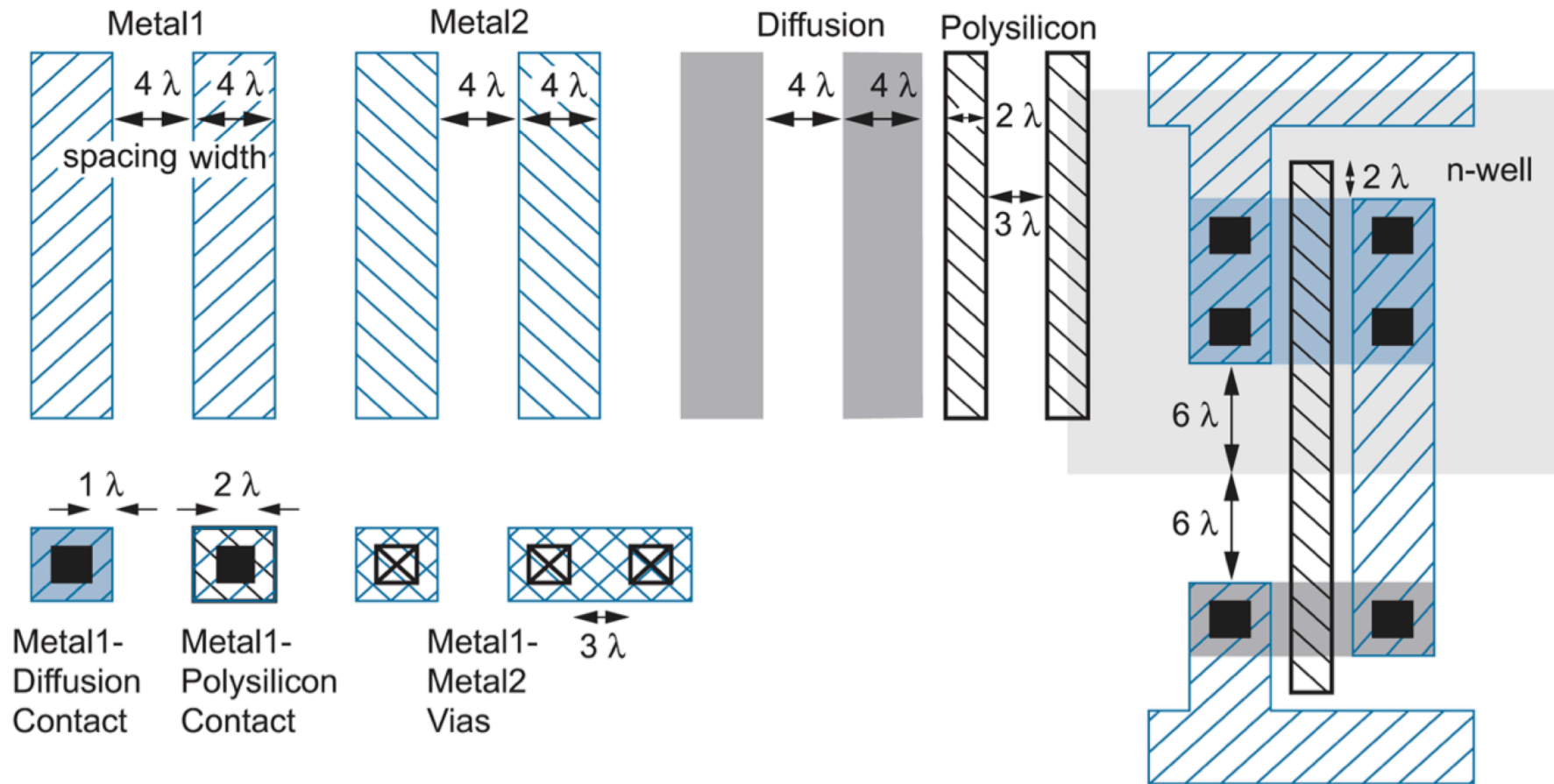- Objective:

maximum yield and minimizing area
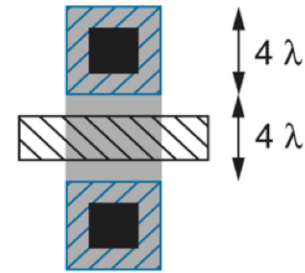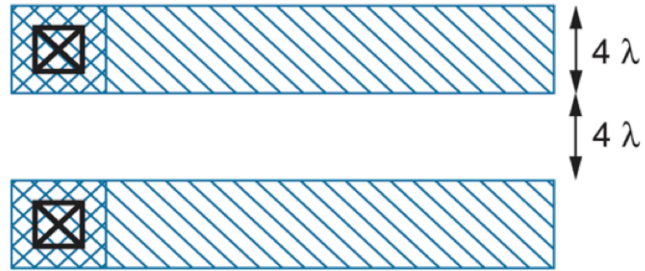
- Rule types
  - Width
  - Spacing
  - Separation
  - Extension
  - Overlap

Design Rules (I)

Basic layout constraints

4λ
4λ

4λ
4λ

(b)

V_{DD}

A   Y

GND

(a)

8/2
4/2

(b)

2
1

(c)

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12
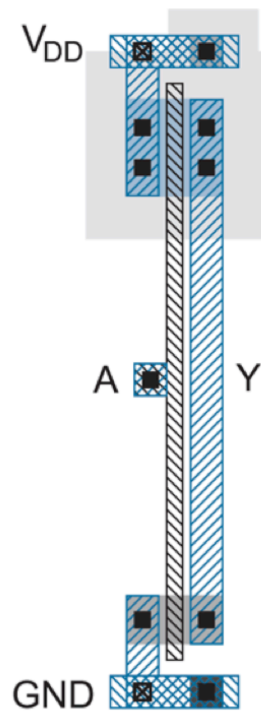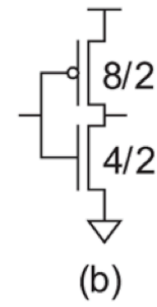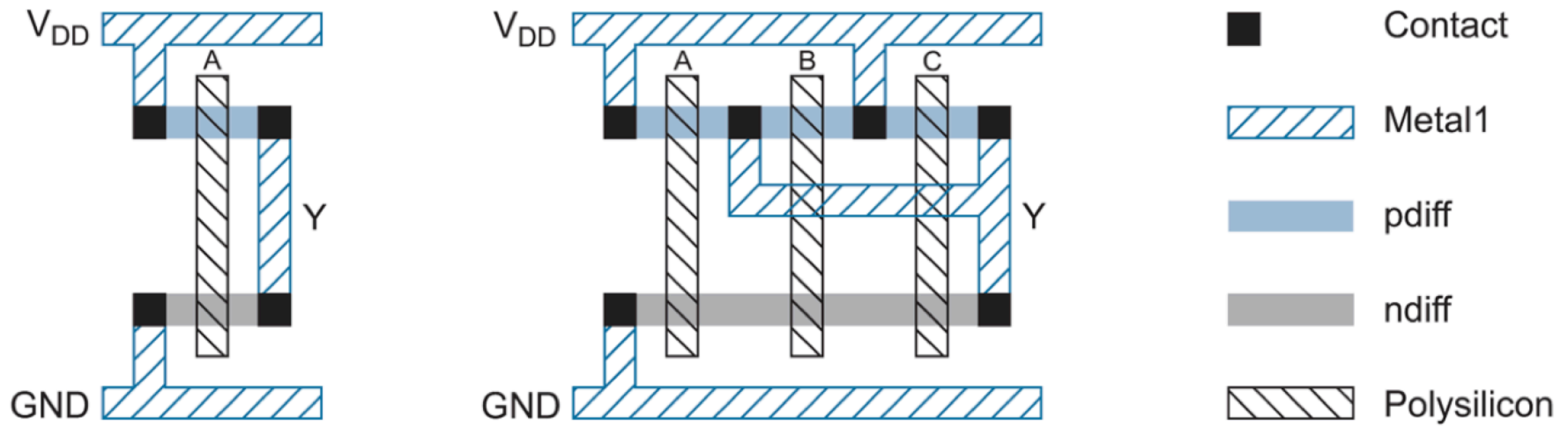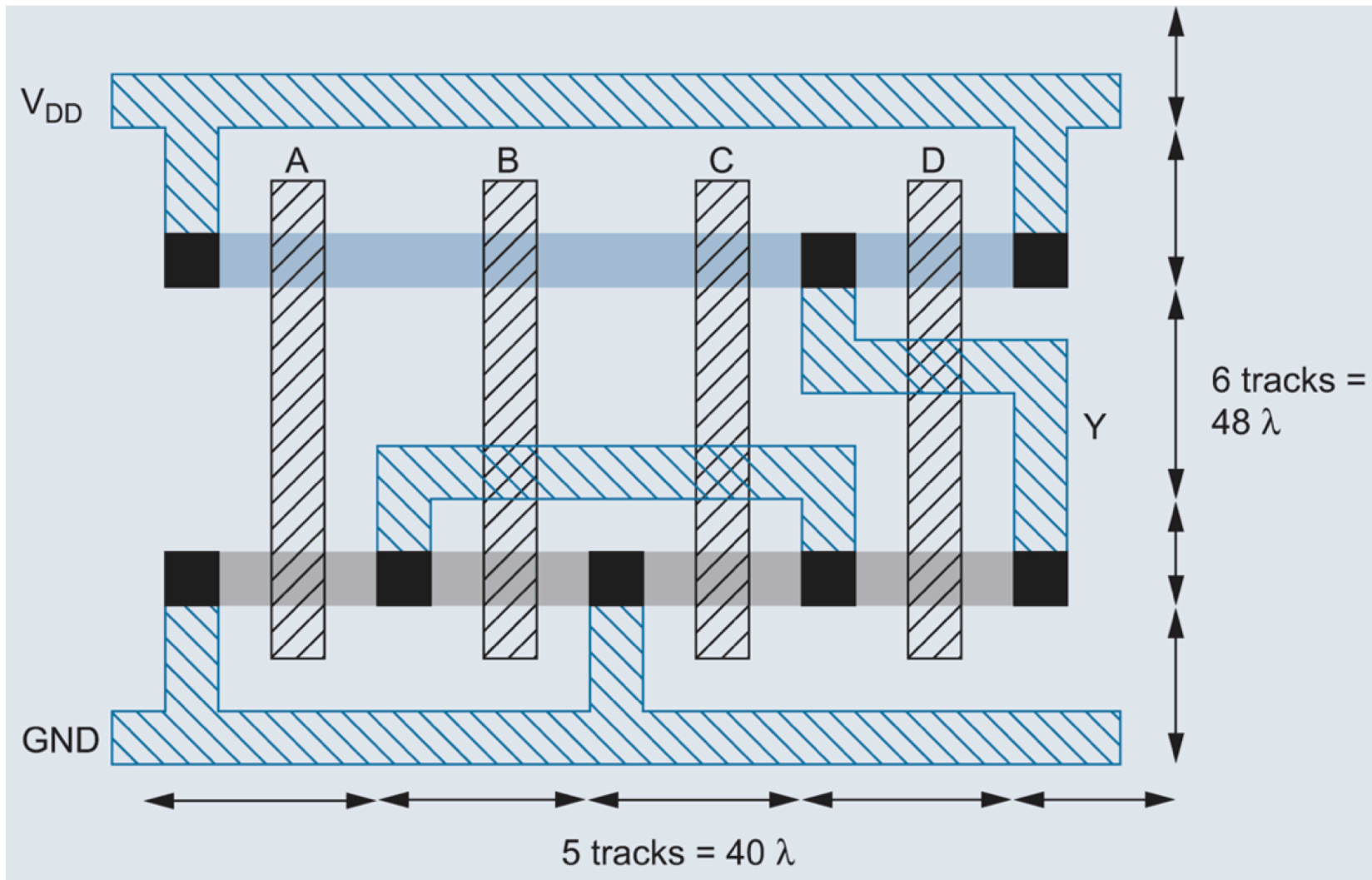
Layout style for libraries –stick diagrams- (I)
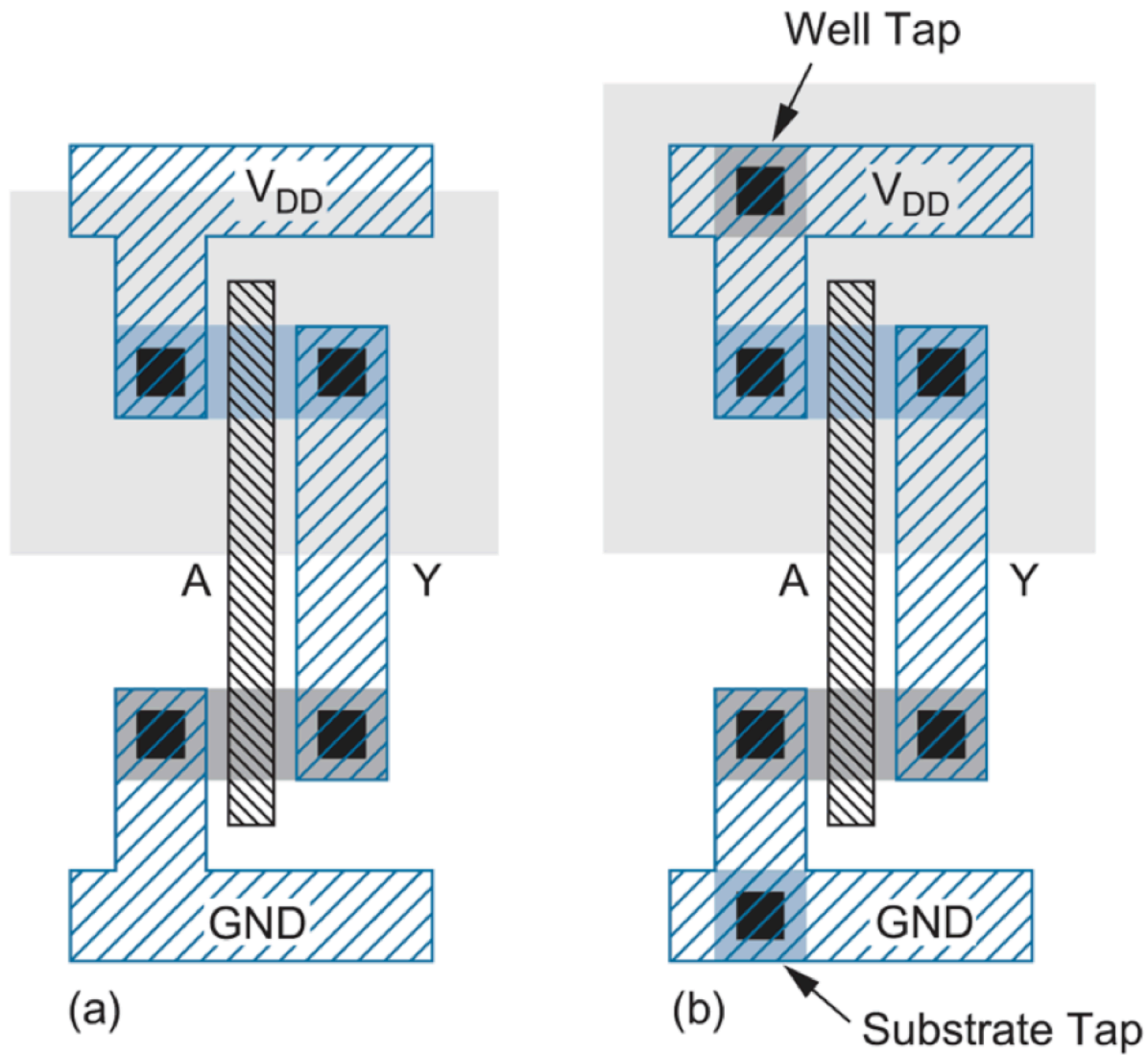

explore with micro-Wind

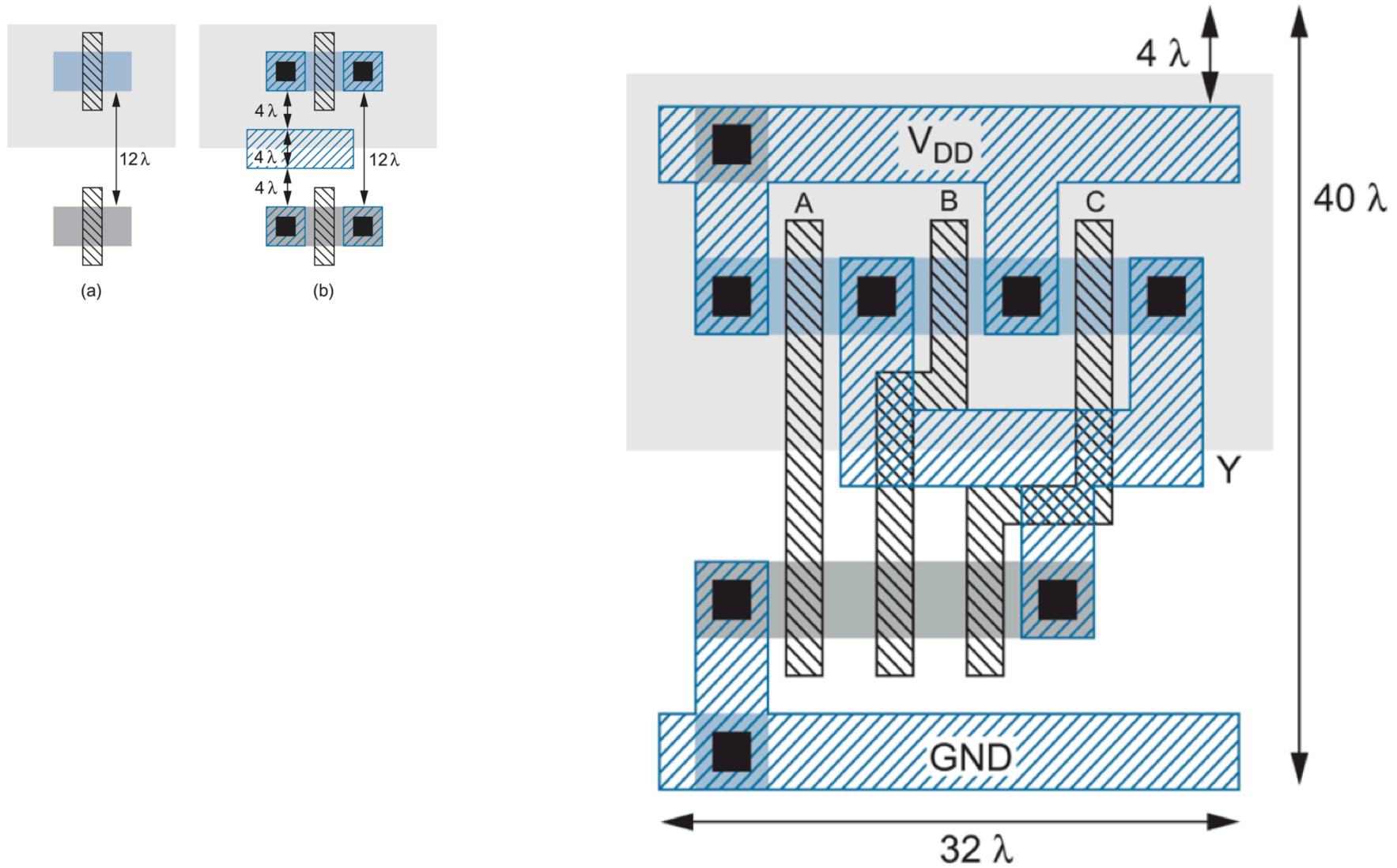# Layout style for libraries –stick diagrams- (II)

explore with micro-Wind

Substrate and well contact –the fourth hidden terminal-

explore with micro-Wind

Layout style for libraries (II)

explore with micro-Wind

Computer Aided Design Tools

DSCH 3

Schematic Modeling
Analog & digital Library models

Digital Simulation | *Verilog Extraction* | *SPICE Extraction*

LTSpice
WindSpice

FPGA Tools

Verilog File

Synthesis

Floorplanning

Place & Route

Programming File

.bit or .ied

Functional Simulation

ModelSim / other

Verilog Compiler ← **Constraints**

nanoLambda Layout Editor ← **Technology rule files**

Analysis
DRC, ERC
Delay Analyzer
Crosstalk Analyzer
2D Cross section
3D Analyzer

Place & Route

Layout Extraction

ProTHUMB
Advance post layout simulator

Layout Conversion *SPICE, CIF*

MICROWIND 3

http://www.microwind.net

IO Cards
Traffic Light Controller, Key Pad, Display (LCD, 7 segs)

FPGA / CPLD Boards

Tape out to FAB. *CIF*

MICROWIND Tool

3rd Party Tools