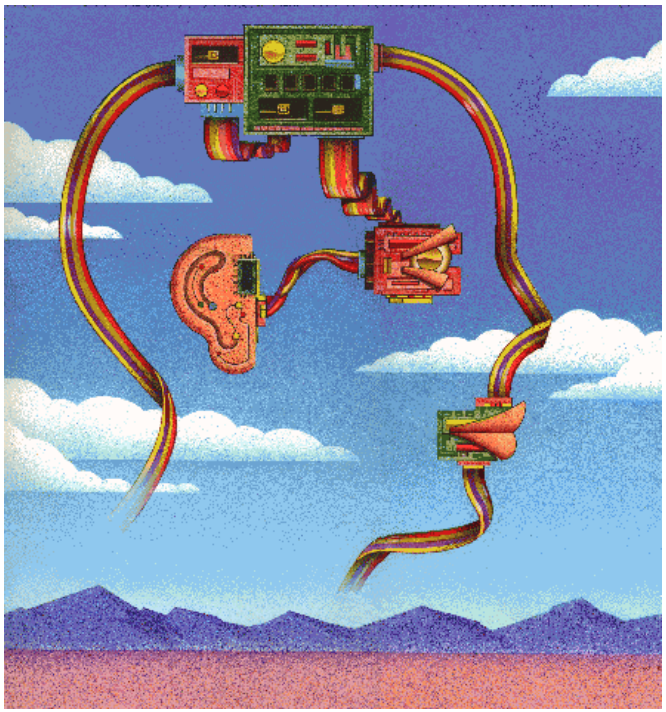

MOS Transistors Models

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The MOS transistor – Levels of Abstraction-

Model Equations

$$If \quad V_{GS} < 0$$
$$I_{DS} = 0$$

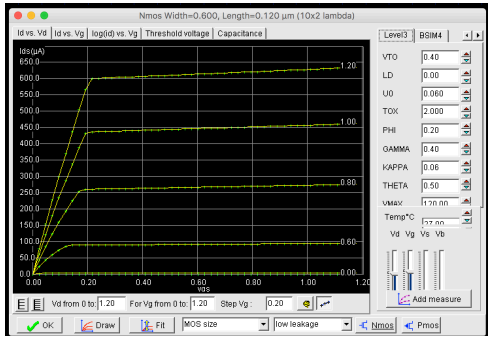
$$If \quad V_{DS} > V_{GS} - V_{TO}$$

$$I_{DS} = \left(\frac{W}{L}\right)\left(\frac{UO}{2}\right)\frac{\varepsilon_0 \varepsilon_r}{TOX}(V_{GS} - V_T)^2$$

$$If \quad V_{DS} < V_{GS} - V_{TO}$$

$$I_{DS} = \left(\frac{W}{L}\right) UO \frac{\varepsilon_0 \varepsilon_r}{TOX}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

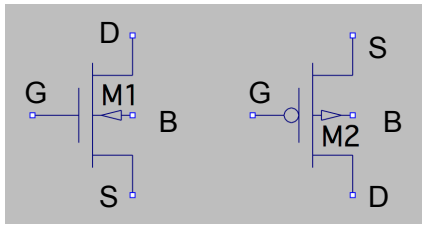
$$V_T = V_{TO} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$



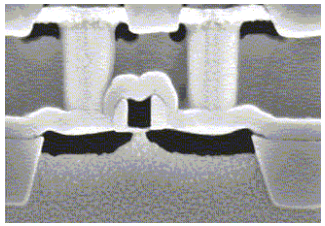
Model Current-Voltage Characteristics

MATHEMATICAL

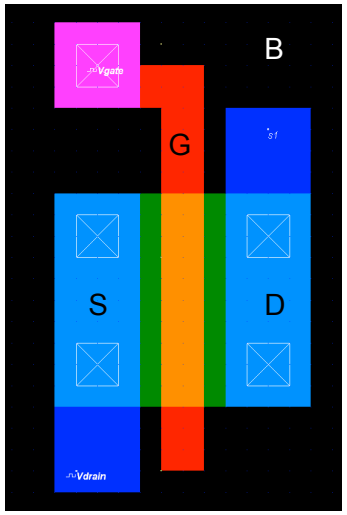
Symbol



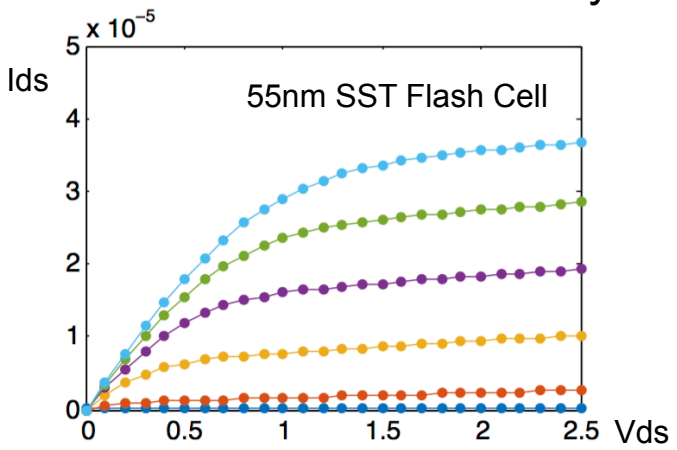
NMOS PMOS



SEM photograph



Layout



Current – Voltage Characteristics

PHYSICAL

What is a model?

1. An intuitive and conceptual abstraction of a complex physical process

2. A mathematical abstraction of a complex physical process that is capable of predicting experimental observations.

What is a MODEL?

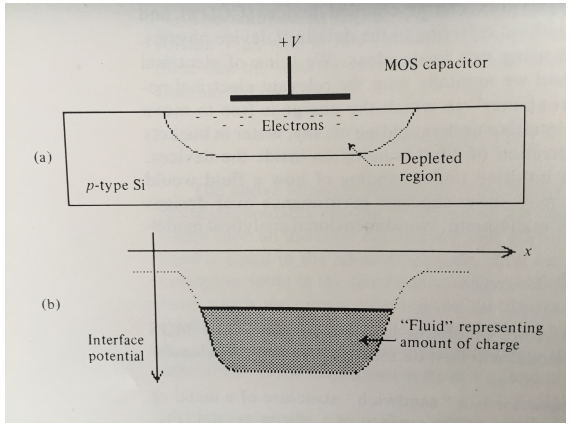
1. An intuitive and conceptual abstraction of a complex physical process

2. A mathematical abstraction of a complex physical process that is capable of predicting experimental observations.

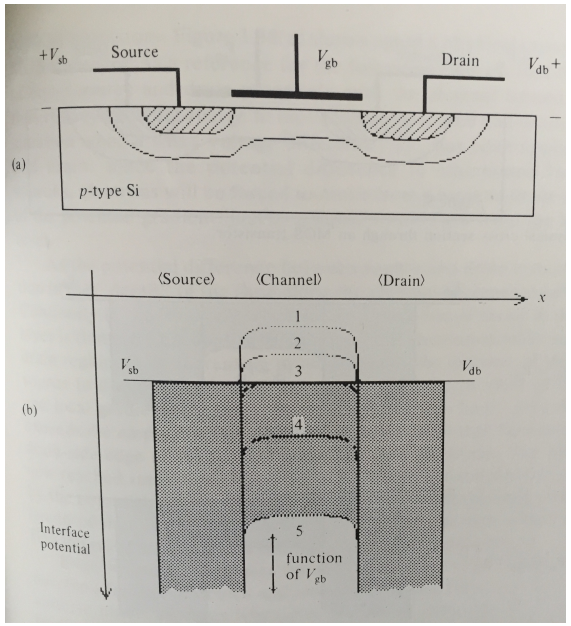
MOS fluidic analogy: a conceptual model (I)

From Mead and Conway

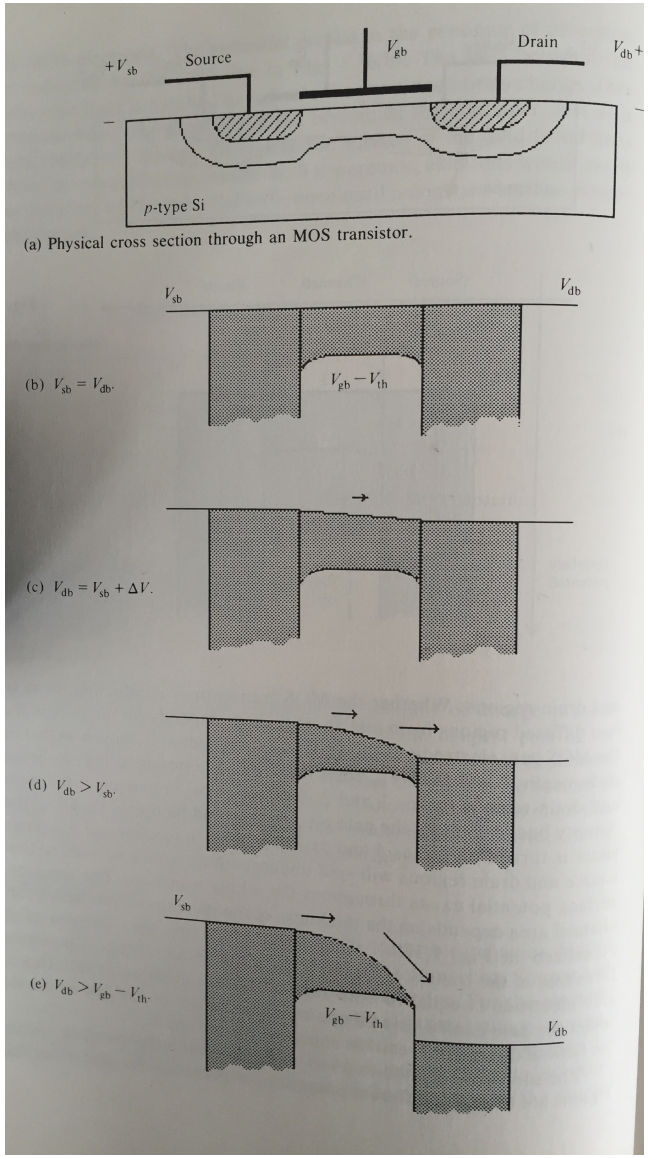
MOS Capacitor



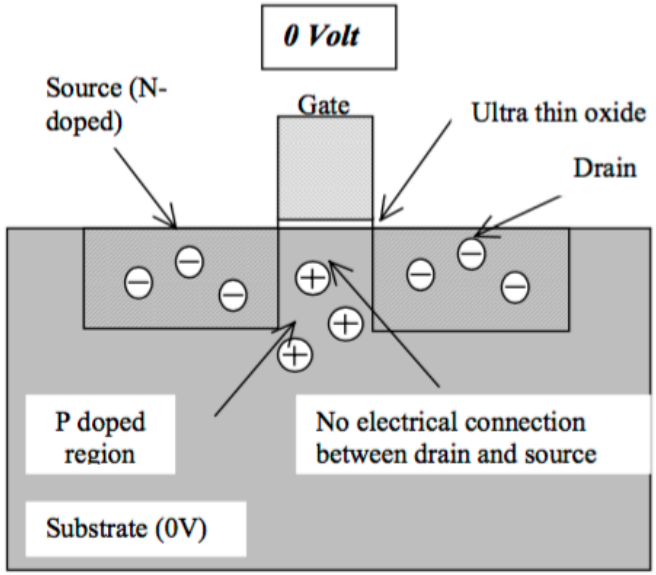
MOS Transistor

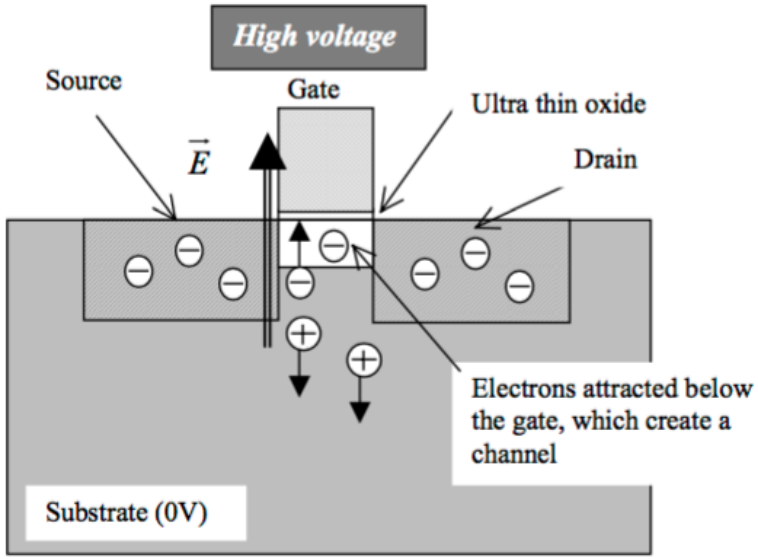


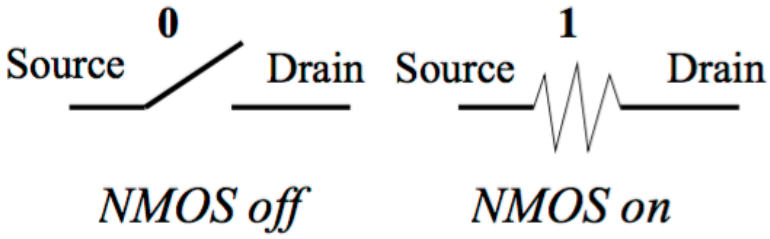
MOS Transistor Varia Bias



NMOS as a switch/resistor: a conceptual model (II)



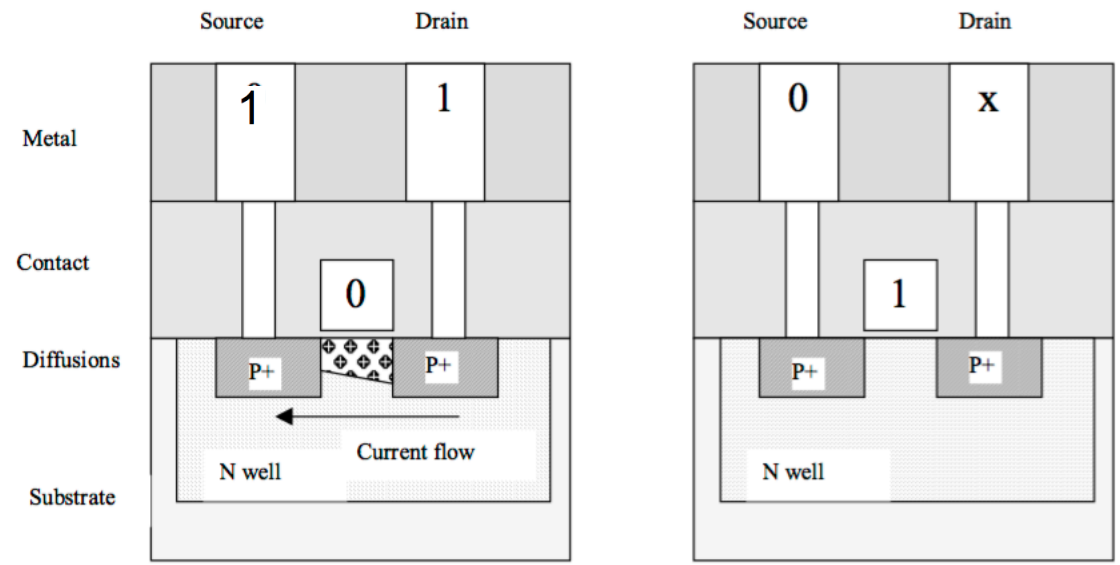


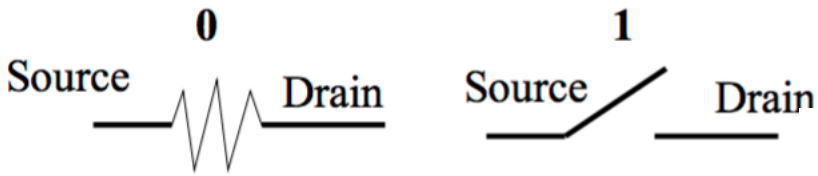


Gate	Source	Drain
0	0	X
0	1	X
1	0	0
1	1	1

not a good one

PMOS as a switch/resistor: a conceptual model (III)

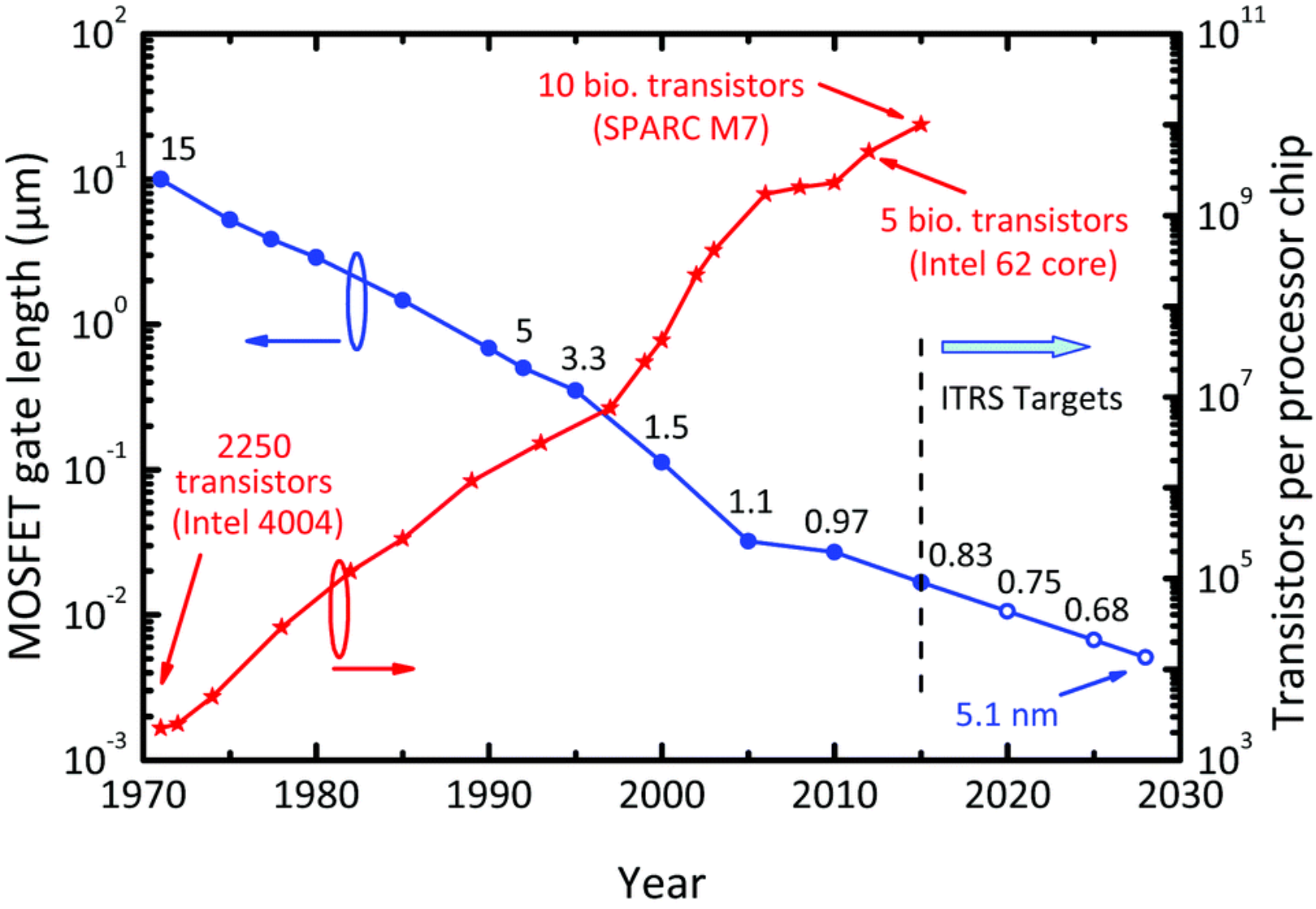




not a good zero

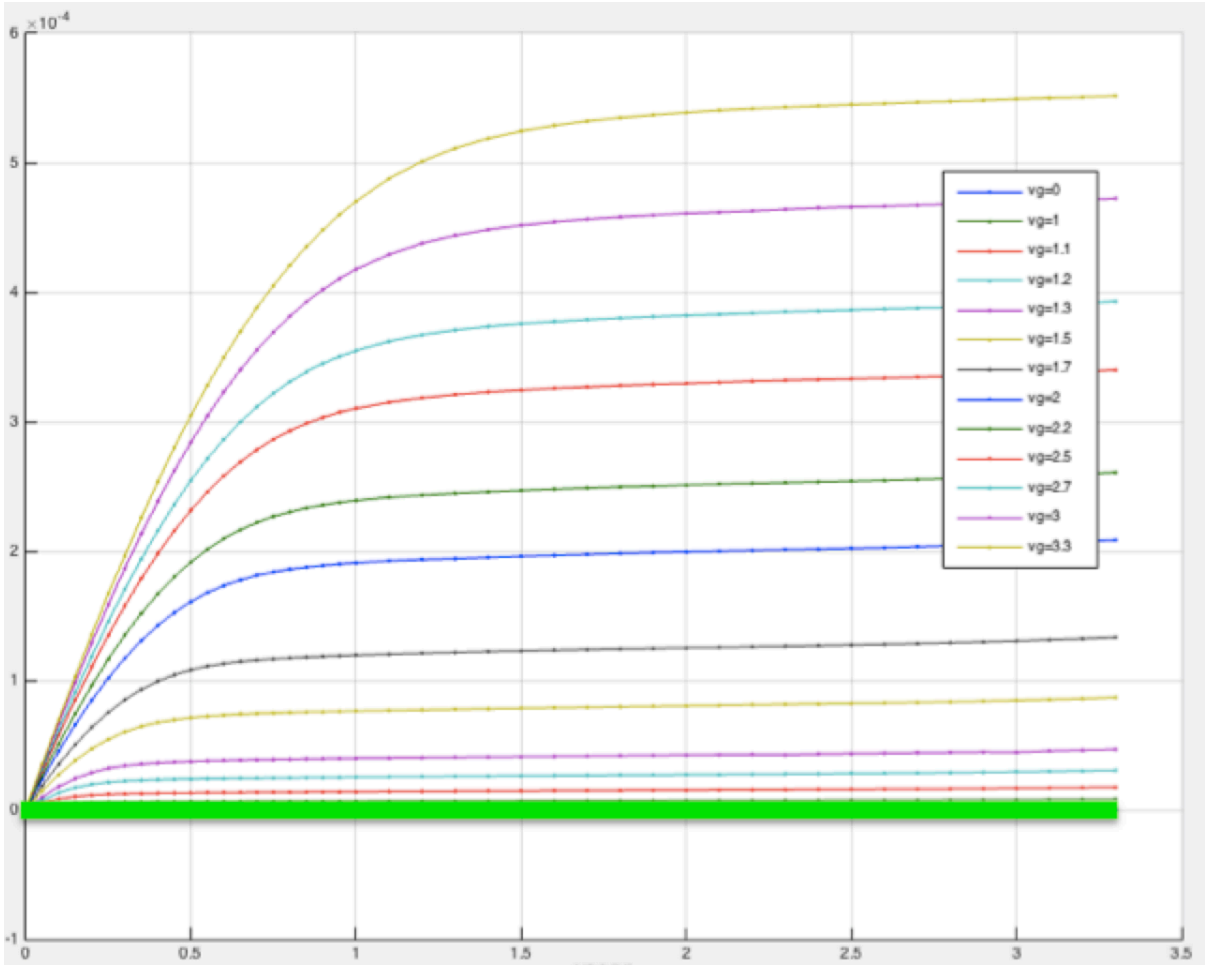
Gate	Source	Drain
0	0	0
0	1	1
1	0	X
1	1	X

What are the physical values for 0 and 1



chip/logic voltages (blue line)

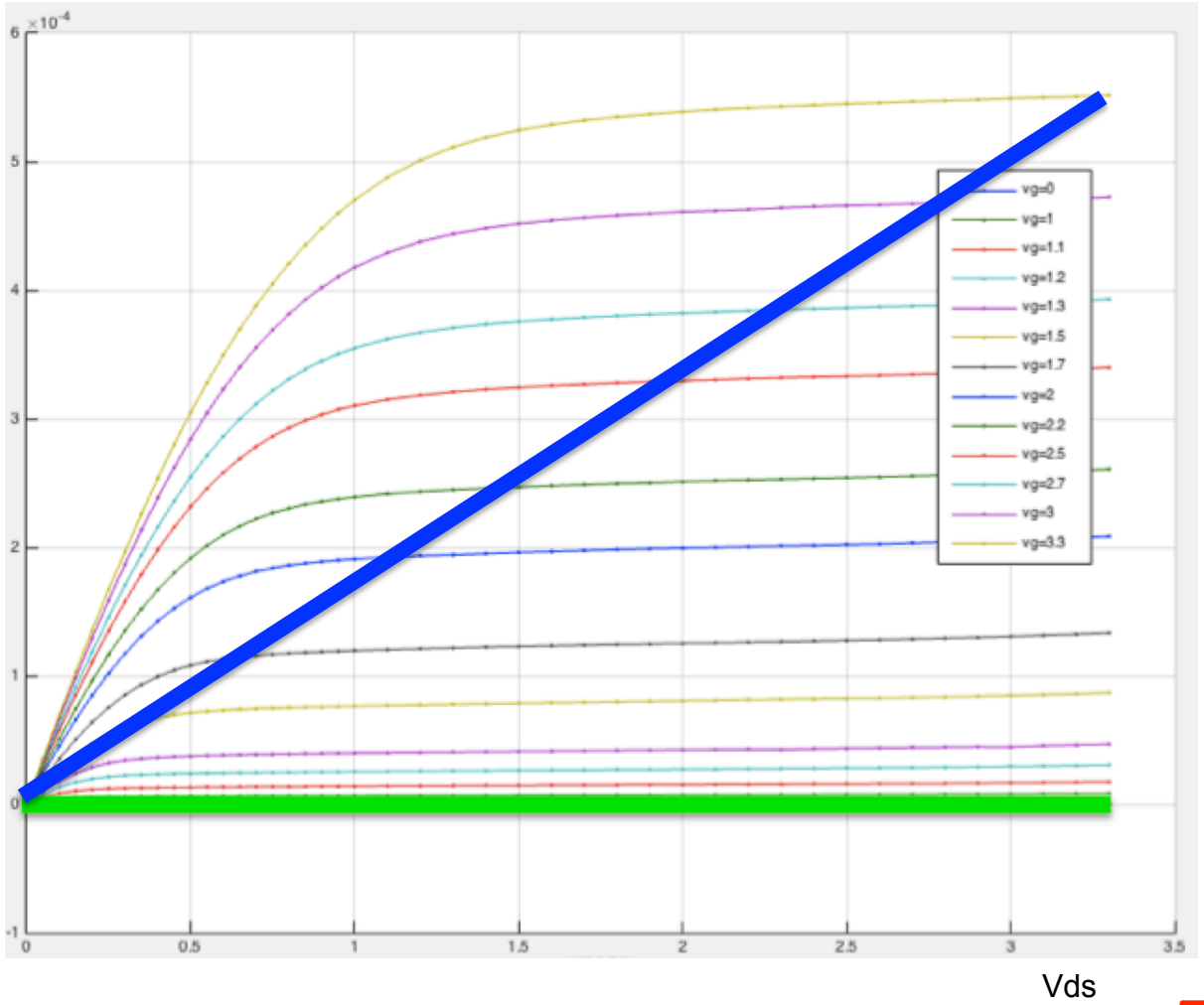
MOS switch model relation to I-V characteristics (I)



180nm technology

With digital input on gate the device is either ON or OFF

MOS switch model relation to I-V characteristics (II)



180nm technology

With digital input on gate the device is either ON or OFF

Approximate ON with the blue line

R_{ON} ~ 3.3 V / 0.55 mA = 6K

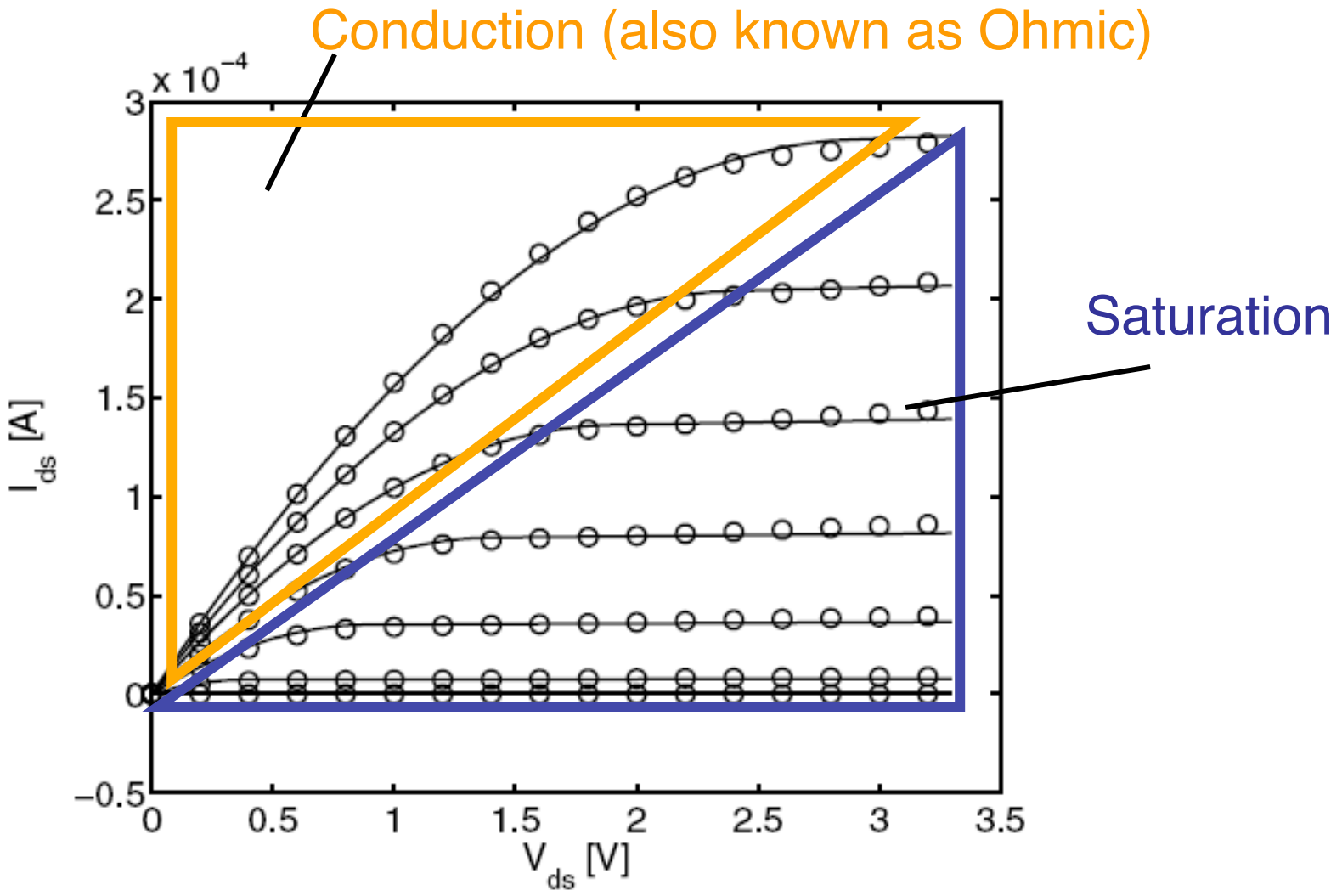
What is a MODEL?

1. An intuitive and conceptual abstraction of a complex physical process

2. A mathematical abstraction of a complex physical process that is capable of predicting experimental observations.

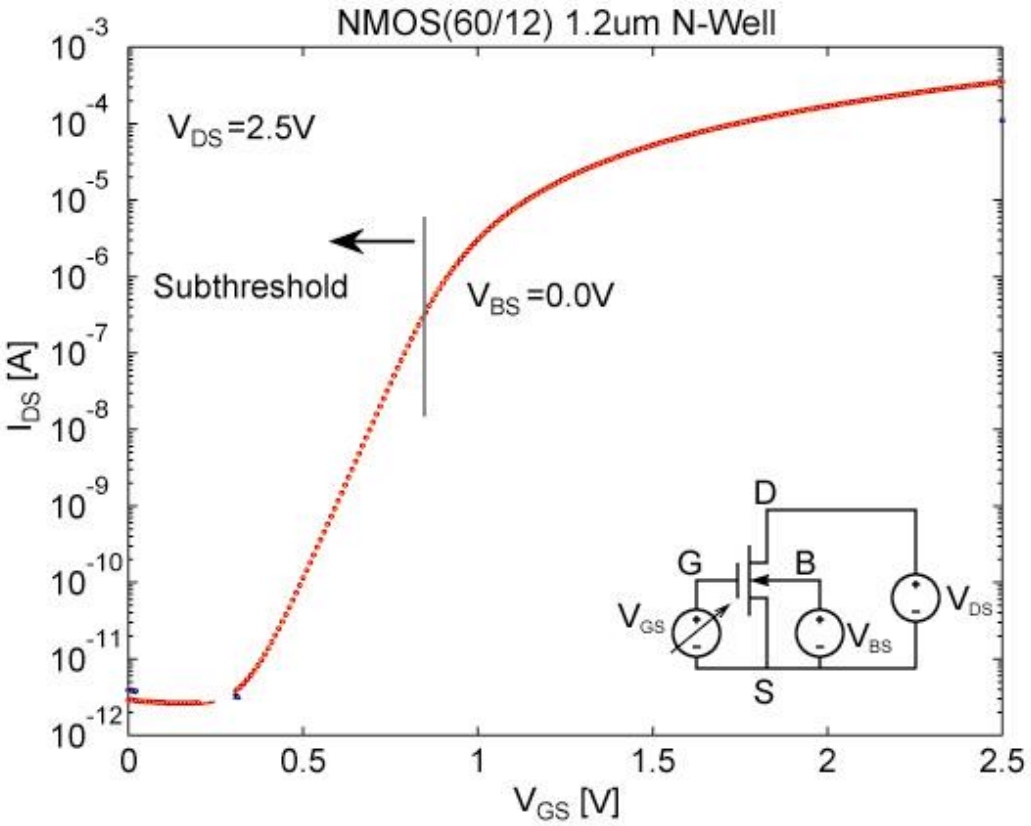
Conduction –ohmic- vs saturation

Device operation characterized by the form of the current as a function of the bias voltage between the DRAIN and the source terminals (Vds)

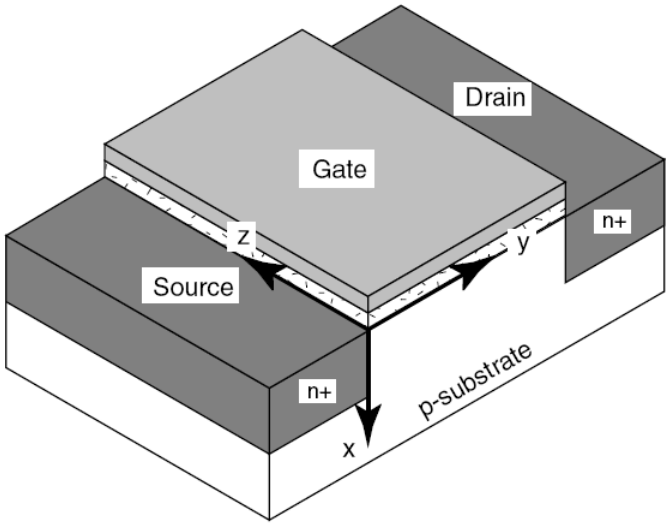


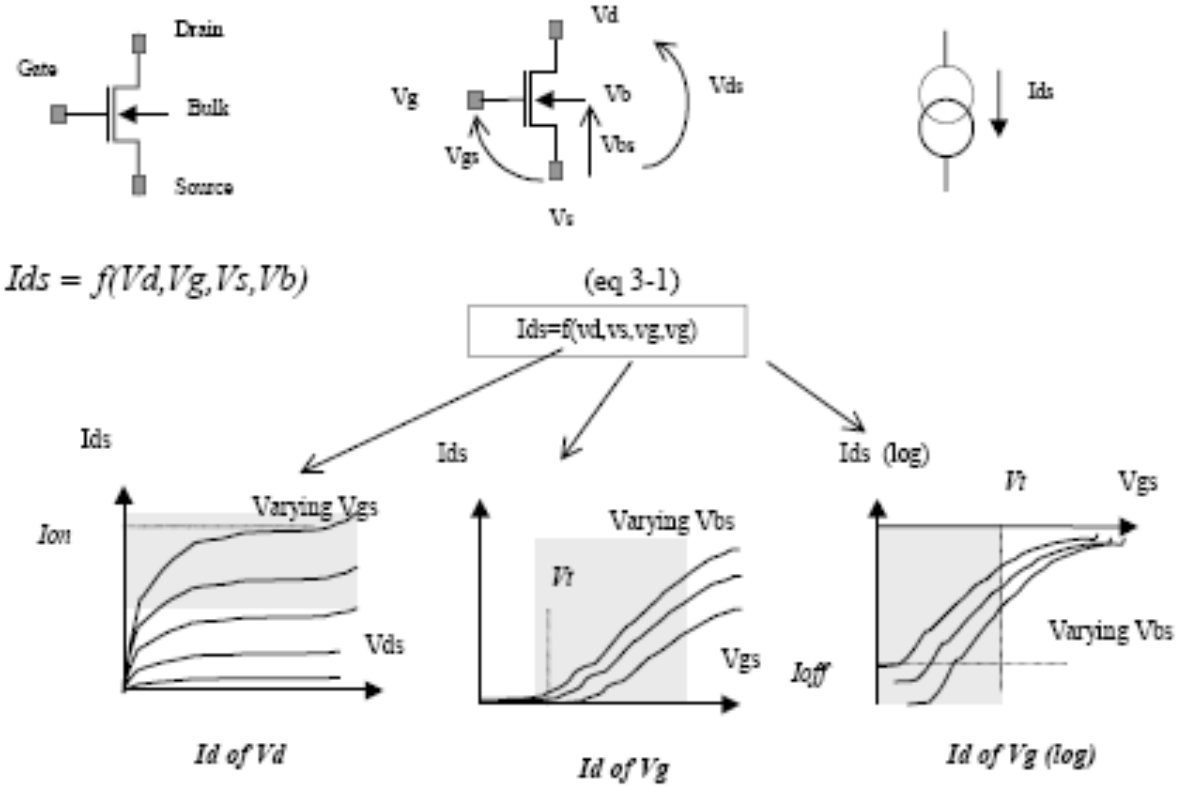
Above threshold vs sub-threshold behaviour

Device operation characterized by the form of the current as a function of the bias voltage between the gate and the source terminals (Vgs)



MOS transistor mathematical model





Mathematical model –above threshold-

$$If \quad V_{GS} < 0$$
$$I_{DS} = 0$$

$$If \quad V_{DS} > V_{GS} - V_{TO}$$

Saturation

$$I_{DS} = \left(\frac{W}{L}\right)\left(\frac{UO}{2}\right)\frac{\varepsilon_0 \varepsilon_r}{TOX}\left(V_{GS} - V_T\right)^2$$

$$If \quad V_{DS} < V_{GS} - V_{TO}$$

Ohmic

$$I_{DS} = \left(\frac{W}{L}\right) UO \frac{\varepsilon_0 \varepsilon_r}{TOX}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$V_T = V_{TO} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

$\varepsilon_0 = 8.85\ 10^{-12}$ F/m is the absolute permittivity

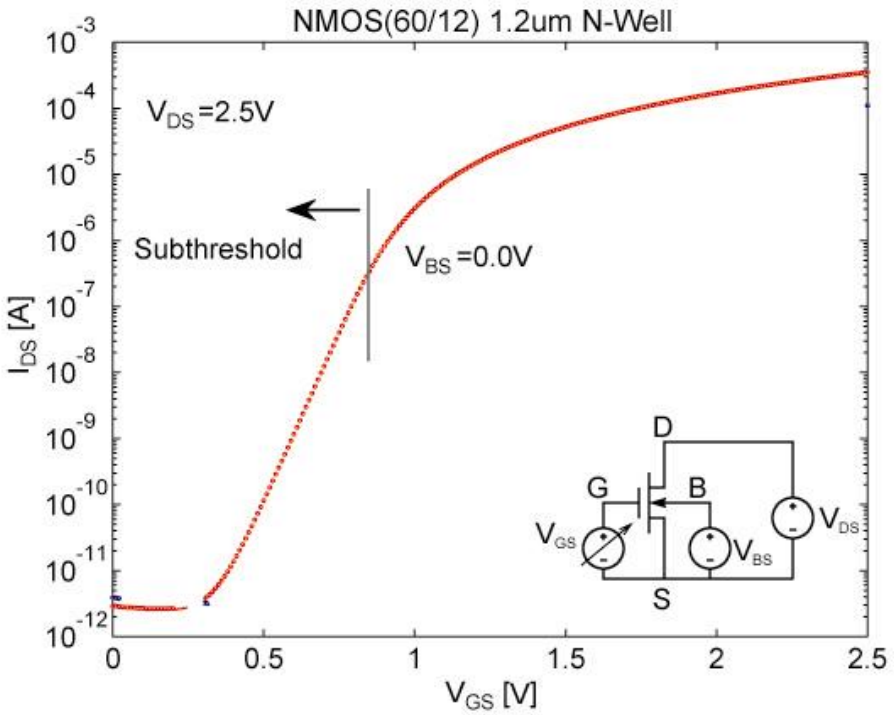
ε_r = relative permittivity, equal to 3.9 in the case of SiO2 (no unit)

Mos Model 1 parameters			
Parameter	Definition	Typical Value 0.12µm NMOS	PMOS
VTO	Theshold voltage	0.4V	-0.4V
U0	Carrier mobility	0.06m^2/V-s	0.02m^2/V-s
TOX	Gate oxide thickness	2nm	2nm
PHI	Surface potential at strong inversion	0.3V	0.3V
GAMMA	Bulk threshold parameter	0.4 V$^{0.5}$	0.4 V$^{0.5}$
W	MOS channel width	1µm	1µm
L	MOS channel length	0.12µm	0.12µm

Model parameters

Above threshold vs sub-threshold behaviour

Device operation characterized by the form of the current as a function of the bias voltage between the gate and the source terminals (Vgs)



Mathematical model –subthreshold-

$$I_D \equiv I_{DS} = S\, I_{n0} \exp\left(\frac{\kappa_n V_{GB}}{V_t}\right)\left[\exp\left(\frac{-V_{SB}}{V_t}\right) - \exp\left(\frac{-V_{DB}}{V_t}\right)\right]$$

$$I_D \equiv I_{SD} = S\, I_{p0} \exp\left(\frac{-\kappa_p V_{GB}}{V_t}\right)\left[\exp\left(\frac{V_{SB}}{V_t}\right) - \exp\left(\frac{V_{DB}}{V_t}\right)\right]$$

$$V_t \equiv \frac{kT}{q} \qquad \kappa \equiv \frac{1}{\eta} \equiv \frac{C_{ox}}{C_{ox} + C_{dep}} \qquad S \equiv \frac{W}{L}$$

Parameters:

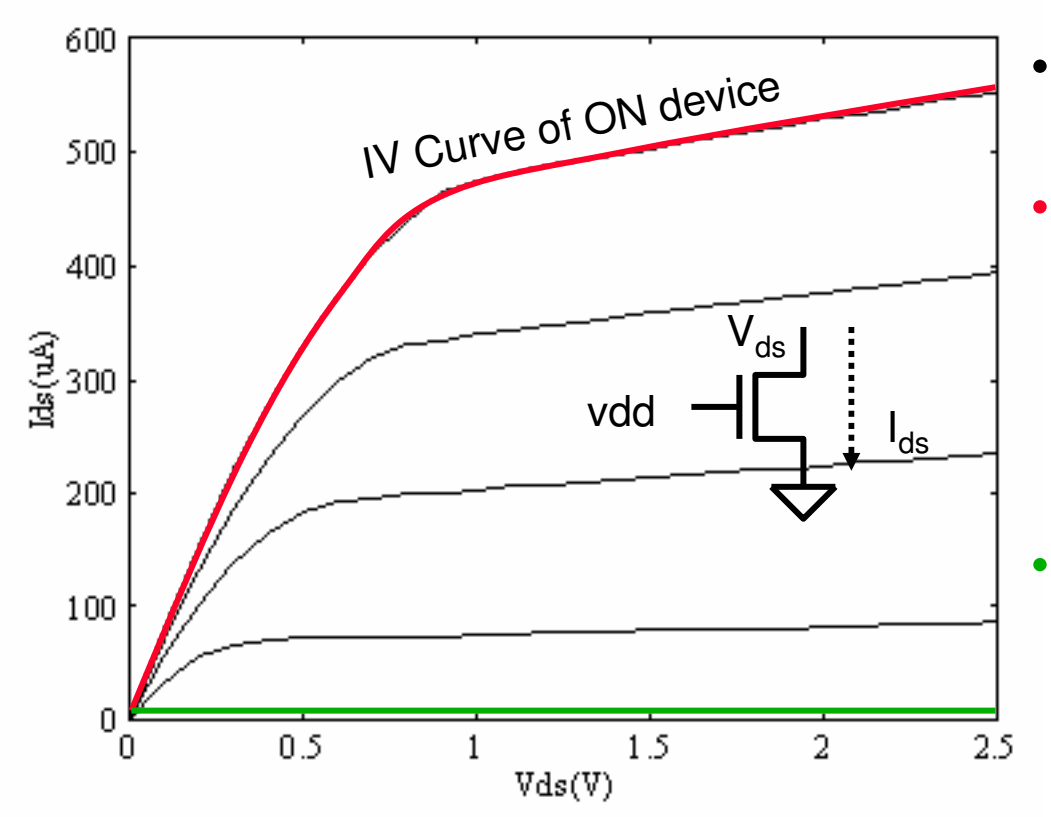
$$I_{p0} = 0.5 \times 10^{-18}\, A$$

$$I_{n0} = 0.9 \times 10^{-18}\, A$$

$$\kappa = 0.7$$

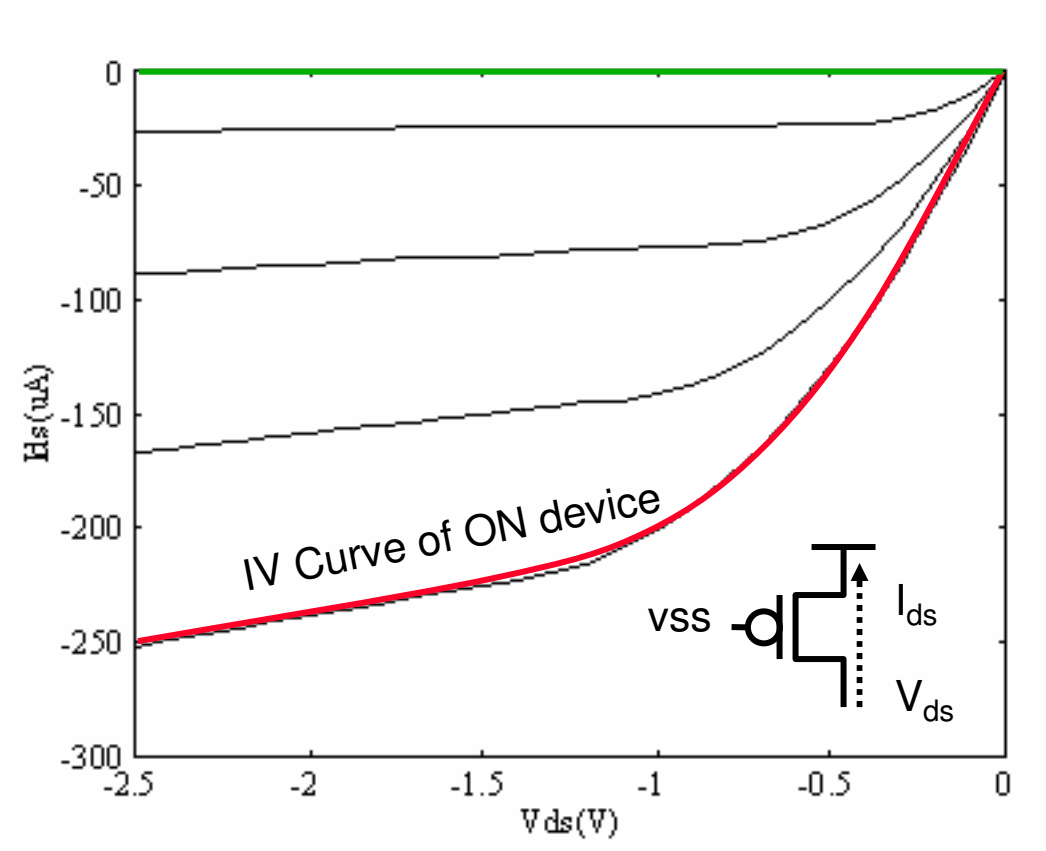
$$V_t = 0.26\, Volts$$

Operating current for an NMOS



- Operates on one of two curves
- on
  - Looks like a current source initially (high V_{ds})
  - Looks like a resistor later (low V_{ds})
- off
  - Open circuit always

Operating current for a PMOS



- Same behavior as NMOS
  - Open circuit when off
  - Current source or resistor when on

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