Making a Chip that Sees
a.k.a. Introduction to VLSI Systems

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economic growth depends on chips
Over the last five decades, advances in semiconductor-based electronics have been incorporated into systems that go well beyond computing per se, impacting sectors ranging from aerospace and entertainment to medicine and manufacturing. We rely on semiconductors in almost every aspect of our lives. Over those fifty years, the ability to reduce the size of the individual transistors by half roughly every 18 months has led to increased performance at lower cost and greater functionality in ever smaller form factors, a trend known as Moore's Law. Semiconductors are the foundation of information technology and have made possible the Internet, online businesses, and social media—connecting people and information across the face of the globe. The information economy is creating vast quantities of data that are growing exponentially; the volume of data created annually is expected to be nearly 30 exabytes by 2017.
mobile data growth

![Graph showing mobile data growth from 2014 to 2019](image_url)

- Exabytes per Month:
  - 2014: 2.5 EB
  - 2015: 4.2 EB
  - 2016: 6.8 EB
  - 2017: 10.7 EB
  - 2018: 16.1 EB
  - 2019: 24.3 EB

Source: Cisco VNI Mobile, 2015
Size reduction in sensors falls within the trend of general compaction of information, communications, and telecommunications (ICT) system scaling known as Bell’s Law, illustrated in Figure 5. For example, the volume of a general-purpose computing unit has scaled down from ~6.53 \times 10^8 \text{ cm}^3 in 1958 (IBM 709) to ~80 \text{ cm}^3 in 2007 (iPhone1) to ~2 \text{ cm}^3 in 2014 (Intel’s Edison chip). A related trend is dramatic unit cost reduction derived in part from an exponential increase in production volume.

Node Characteristics

An individual sensor node should include components for transduction, computation, memory, communication, and power supply. Nodes may need to act autonomously, be programmable via the network to increase flexibility, and support communication with other network nodes—all while maintaining security and privacy. In many applications, nodes will be embedded in the environment and should not interfere with other functionality. Moreover, many autonomous nodes will be constrained by size and energy; therefore smart energy management will be needed, for example, to support periodic bursts of operation. In the case of small-scale "nano-nodes" that are not connected to external power, the available volume for onboard energy storage will be extremely limited. The smallest node that has been reported is ~ 10 mm^3, and the challenging target of demonstrating a fully operational node 1 mm^3 in size has yet to be achieved. A nearer-term application driver could be intelligent image sensors with full scale communication capabilities. It should be noted that while the scaling limits of individual electronic devices have been estimated from physics-based considerations, the question of how small a system can be and still offer useful functionality remains open. Research is needed to understand the possible physics-based estimates for the smallest-size intelligent sensor nodes.

Rebooting the IT Revolution: A Call to Action, SRC, Sept 2015
computers and the brain

Mammalian Brains vs Computers

- Parallel distributed architecture
- Low power (25W), small footprint (1 liter)
- Asynchronous (no global clock)
- Analog computing, Digital communication
- Integrated memory and computation
- Intelligence via Learning thru BBE interactions
- Composed of noisy components and operates at low speeds (< 10 Hz)
- Spontaneously active

- Serial architecture
- High power (100MW), Large footprint (40M liters)
- Synchronous (global clock)
- Digital computing and communication
- Memory and Computation are clearly separated
- Intelligence via programmed algorithms/rules
- Precision in components and operates at very high speeds (GHz)
- No activity unless instructed

Rebooting the IT Revolution: A Call to Action, SRC, Sept 2015
Back in the 50s

Jack Kilby, Texas Instruments, Phase Shift Oscillator (1958)

The Nobel Prize in Physics 2000

Zhores I. Alferov
Prize share: 1/4

Herbert Kroemer
Prize share: 1/4

Jack S. Kilby
Prize share: 1/2

The Nobel Prize in Physics 2000 was awarded “for basic work on information and communication technology” with one half jointly to Zhores I. Alferov and Herbert Kroemer “for developing semiconductor heterostructures used in high-speed- and opto-electronics” and the other half to Jack S. Kilby “for his part in the invention of the integrated circuit”.

Robert Noyce, Fairchild/Intel Integrated Circuit (1959)

Google Doodle December 12, 2011
Back in the 70s

The Nobel Prize in Physics 2009

The Nobel Prize in Physics 2009 was divided, one half awarded to Charles Kuen Kao "for groundbreaking achievements concerning the transmission of light in fibers for optical communication", the other half jointly to Willard S. Boyle and George E. Smith "for the invention of an imaging semiconductor circuit - the CCD sensor".

Scientific background on the Nobel prize in Physics 2009
Moore’s law

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Electronics, Volume 38, Number 8, April 19, 1965

1. More transistors per unit silicon area
2. Lower energy costs for computation
80s-90s: the heydays of CAD and foundry design
So how do fabricate our own chips?

**Key idea:** Use a number of different manufacturers to contribute manufacturing capacity to multiuser projects.

- ON Semiconductor 500 nanometer CMOS
- TSMC 180, 130, 90, 65, 45, 28 nanometer CMOS
- GF 180, 130, 55, 45 nanometer BiCMOS
- IBM 45 nanometer SOI CMOS!

http://www.mosis.org/
As integrated circuits get smaller and cheaper, they become more ubiquitous, embedded in myriad systems and objects—adding “intelligence” by sensing, communicating, and actuation. They also are increasingly networked, creating the so-called “Internet of Things” (IoT). There are currently an estimated 50 billion sensors connected to objects that are part of the IoT. Some 14 billion of these already are collecting and sending data on the Internet; by 2020, there are expected to be 32 billion connected devices.

At the same time, the capabilities of leading-edge high performance computing systems continue to increase. These powerful machines combine large numbers of the fastest processors to address challenges previously beyond reach. High performance computers are used extensively in applications as varied as nuclear stockpile stewardship, weather prediction, forest fire management, and fundamental materials research. Areas of intense interest and research today are data analytics and machine learning. Advances in these fields transform massive amounts of data into insights used to predict, anticipate, inform, and advise.

The convergence of these trends poses both opportunities and challenges at the infrastructure level. “Insight technologies” include everything from intelligent sensor nodes to scalable data centers. Delivering both efficiency and performance in these technologies will require a hierarchical, tiered architecture. This new IT infrastructure also will require advances in wireless communication hardware. And at every level, there must be appropriate security, privacy, and assurance.

The sections that follow describe essential components of the next IT revolution, that is, the insight technology revolution.

**Intelligent Sensor Nodes**

Sensor technologies are experiencing exponential growth, with future volumes driven by applications not yet envisioned, as depicted in Figure 4.

![Trillion Sensor Visions](image)

**Fig. 4. Forecasts by various organizations for increases in the number of sensors deployed per year.**

“Abundance”
- QCOM Swarm Lab, UCB
- Bosch
- Hewlett-Packard
- Intel
- TI Internet devices

Yole MEMS Forecast, 2012
- 10 year slope
- Mobile Sensors Explosion

T Sensors Bryzek’s Vision
Late 90s CCD to CMOS: the paradigm shift in camera technologies

CCD state of the art
Full 6 inch wafer
111,000,000 pixels
1 frame per second!

Semiconductor Technology Associates
CMOS APS Cameras

1,200,000 / 8,000,000 pixels
$1 / $15

20,000,000 pixels
$200

120,000,000 pixels
$1,000,000
CMOS-APS and digital

Pixel:
- amplification (A)
- quantization (A/D)
- local asynchronous integration
- gain and offset correction

Periphery:
- column intensity accumulator (CAC)
- global intensity accumulator (GAC)
- asynchronous readout (AR)
- global control (GC)

Andreas G. Andreou  Sensors Unlimited  05/13/14
combining silicon rods and cones in a single pixel, with event based asynchronous readout

Santiago Ramon y Cajal

~ 250 μm
unpublished results from first silicon (Tezzaron 130nm 3D-CMOS)
Multivariate Function Approximator Chip in 3D CMOS

A Scalable and Programmable Simplicial CNN
Digital Pixel Processor Architecture

Pablo S. Mandolesi, Member, IEEE, Pedro Julián, Member, IEEE, and Andreas G. Andreou, Member, IEEE
Tezzaron 3D-CMOS Tier 1:
Tezzaron 3D-CMOS Tier 2:
unpublished results from first silicon

TABLE IV: a) Captured image b)Binarization c)Block recognition

TABLE V: a) Border recognition b) Median Filter c) Dilation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>130nm</td>
</tr>
<tr>
<td>Die Size</td>
<td>2x2.5mm²</td>
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<tr>
<td>Cell Size</td>
<td>25x25 μm²</td>
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<tr>
<td>Resolution</td>
<td>48 × 32</td>
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<tr>
<td>Photodiode Type</td>
<td>n+/p-Substrate</td>
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<tr>
<td>Power Supply</td>
<td>1.5V</td>
</tr>
</tbody>
</table>

Example: Counting objects in an image, by using a bounding box and erosion without figure elimination.

%%Capture Image
:BOUNDING
LOAD FUNCTION_F(Bounding)
LOAD FUNCTION_G(Zeros)
Conf = "00000001" ;Border="0", Nei=+, FoG=OR
CNNProcess(CNN, Conf)
WAIT until CNNProcess end
LOAD Counter_on_U
IF image_X = image_U
  goto REDUCE
else
  LOAD Counter_on_X
  goto BOUNDING
end
:REDUCE
repeat 24
LOAD FUNCTION_F(Point_Reduction)
LOAD FUNCTION_G(Zeros)
Conf = "00000001" ;Border="0", Nei=+, FoG=OR
CNNProcess(CNN, Conf)
WAIT until CNNProcess end
LOAD Counter_on_X
end
%Count all the pixels
RST Integrator
for ind=0:47
  COL = ind
  INTEGRATE
end
SELBUSOUT (INTEGER)
520.216 and her friends

- Introduction to MEMS
- CAD Design of Digital VLSI
- Mixed Mode VLSI Systems
- Electronics Design Lab
- Seminar on Large Scale Analog Computation
- FPGA Synthesis Lab
- Introduction to Microfabrication
- MEMS
- More to come; stay tuned!
Life after Intro VLSI course (I)

Tyson Tuttle
Chief Executive Officer

Mr. Tuttle joined Silicon Labs in 1997 and helped design the company's first product, a silicon DAA, that subsequently achieved market share leadership in PC modems and allowed the company to go public in 2000. Mr. Tuttle led the marketing effort behind the company's first RF transceiver products for mobile handsets. He also spearheaded the development and market penetration strategy of the company's successful radio and TV tuner ICs, creating the broadcast business that today represents about one third of the company. Mr. Tuttle led the broadcast product lines until 2010 when the R&D team was consolidated under his leadership as chief technology officer. He then took over as chief operating officer in 2011 and was responsible for managing all of the company's business units and R&D. He became the CEO in 2012. Prior to joining Silicon Labs, Mr. Tuttle held senior design engineering positions at Crystal Semiconductor/Cirrus Logic and Broadcom Corporation. Mr. Tuttle holds an M.S. in electrical engineering from UCLA and a B.S. in electrical engineering from Johns Hopkins University. He has 70 patents issued or pending in the areas of RF and mixed-signal IC design.
Kewei Yang
Chairman and CEO

Throughout his career, Kewei Yang has focused on high-speed analog and mixed-signal design. Before co-founding Analogix, he was vice-president of engineering at Mindspeed, a division of Conexant, where he directed the company's development of high-speed transceivers and switch fabric ICs.
He came to Conexant via its acquisition of HotRail, where he served as chief scientist. He also served as a lead designer at Rendition, a graphics chip company, and at Hewlett-Packard in the Computer Technology Lab.

Yang has a B.S. degree in electrical engineering from Tsinghua University and an M.S. degree in electrical engineering and Ph.D. from Johns Hopkins University.
This could be you!

CEO of Johns Hopkins on the Chip

Johns Hopkins on the chip: microsystems and cognitive machines for sustainable, affordable, personalised medicine and healthcare

A.G. Andreou

Semiconductor technology is contributing to the advancement of biotechnology, medicine and healthcare delivery in ways that it was never envisioned – from chip micro-arrays, to scientific grade CMOS imagers and ion sensing arrays to implantable prostheses. This exponential growth of sensory microsystems has led to an exponential growth of data. Cognitive machines, i.e. advanced computer architectures and algorithms, are carefully co-designed to extract knowledge from such health data making rational decisions and recommendations for therapies. Nano, micro and macro robotics, driven by sophisticated algorithms interface to the human body at different levels and scales, from nano-scale molecules to micron-scale cells to networks and all the way to the scale of organisms. The present era is one where semiconductor technology and the ‘chip’ is the foundation of sustainable and affordable personalised medicine and healthcare delivery.
520.216 will teach you how to go from a simple idea to a system, a CMOS camera chip. You will do analysis, design and finally layout and simulation and fabricate your own chip!

Emphasis is in physical design principles.
Computer Aided Design Tools

MICROWIND Tool Design Flow

Contact:
Sales: sales@microwind.net
Support: support@microwind.net

SPICE Simulator
(3rd Party)

Schematic Modeling
Analog & digital Library models

Digital Simulation
Verilog Extraction
SPICE Extraction

DSCH 3

Verilog File
ModelSim / other

Synthesis
Floorplanning
Place & Route
Programming File
.bit or .led

Verilog Compiler
nanoLambda
Layout Editor

Constraints

Technology rule files

Analysis
DRC, ERC
Delay Analyzer
Crosstalk Analyzer
2D Cross section
3D Analyzer

Place & Route
Layout Extraction
ProTHUMB
Advance post layout simulator

Layout Conversion
SPICE, CIF

Tape out to FAB, CIF

FPGA Tools

FPGA / CPLD Boards

IO Cards
Traffic Light Controller, Key Pad, Display (LCD, 7 segs)

3rd Party Tools

http://www.microwind.net