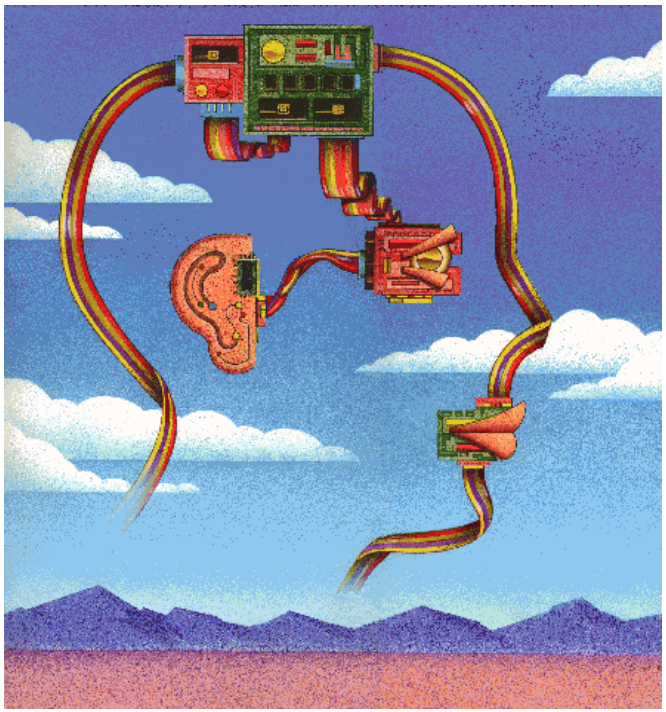
Digital abstraction: MOS abstraction as switch – CMOS Inverter-



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http://andreoulab.net

Levels of Abstraction –MOS switch and Inverter-

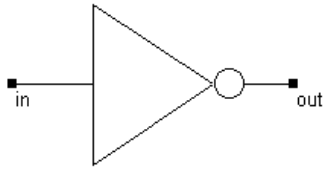
Out = NOT (In)

Out = ~ (In)

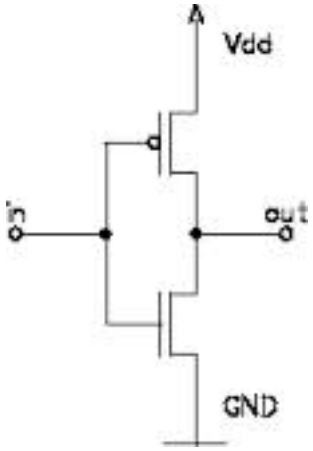
Equation

In	Out
0	1
1	0
X	X

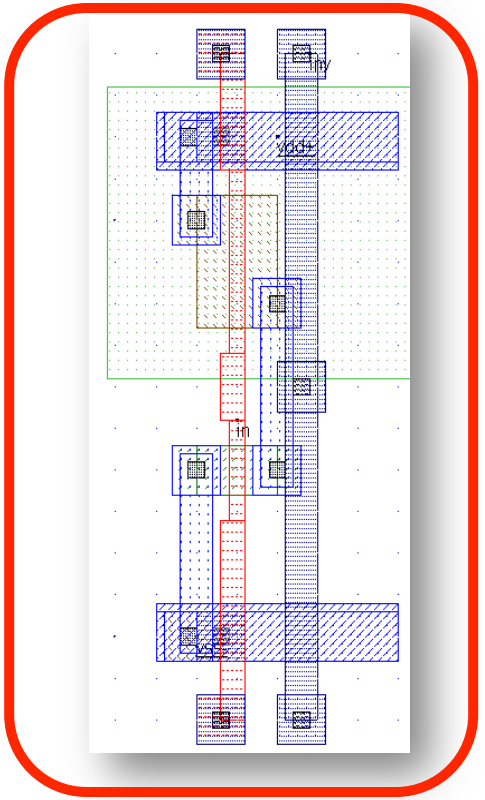
Truth Table



Symbol

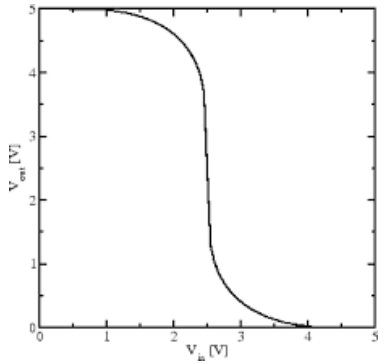


Circuit



Layout

Voltage Transfer Characteristics (VTC)



LOGICAL PHYSICAL

The digital abstraction (I)

from Lecture 2 in MIT 6.004 Computation Structures http://6004.csail.mit.edu/

Concrete encoding of information

We can build upon almost any physical phenomenon…

~~lanterns~~

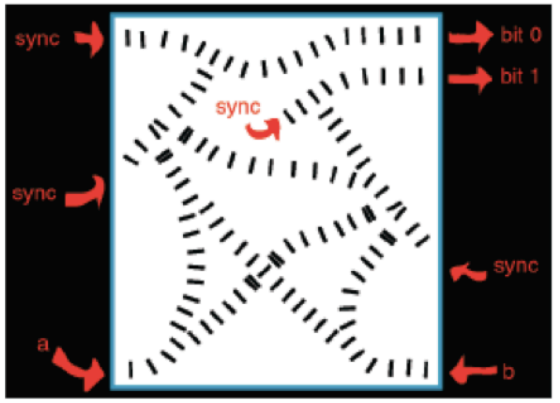
~~dominos~~

~~engraved stone tablets~~

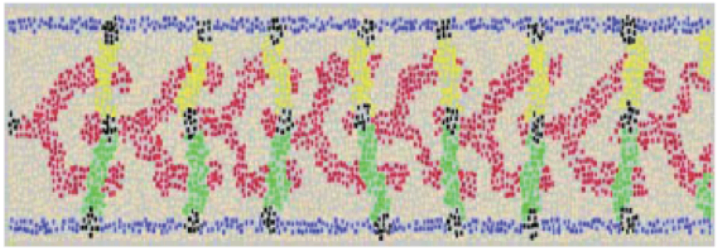
~~Billiard balls~~

~~E. Coli~~

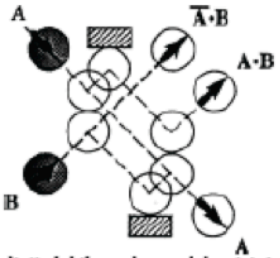
~~polarization of a photon~~



http://www.pinkandaint.com/oldhome/comp/dominoes/



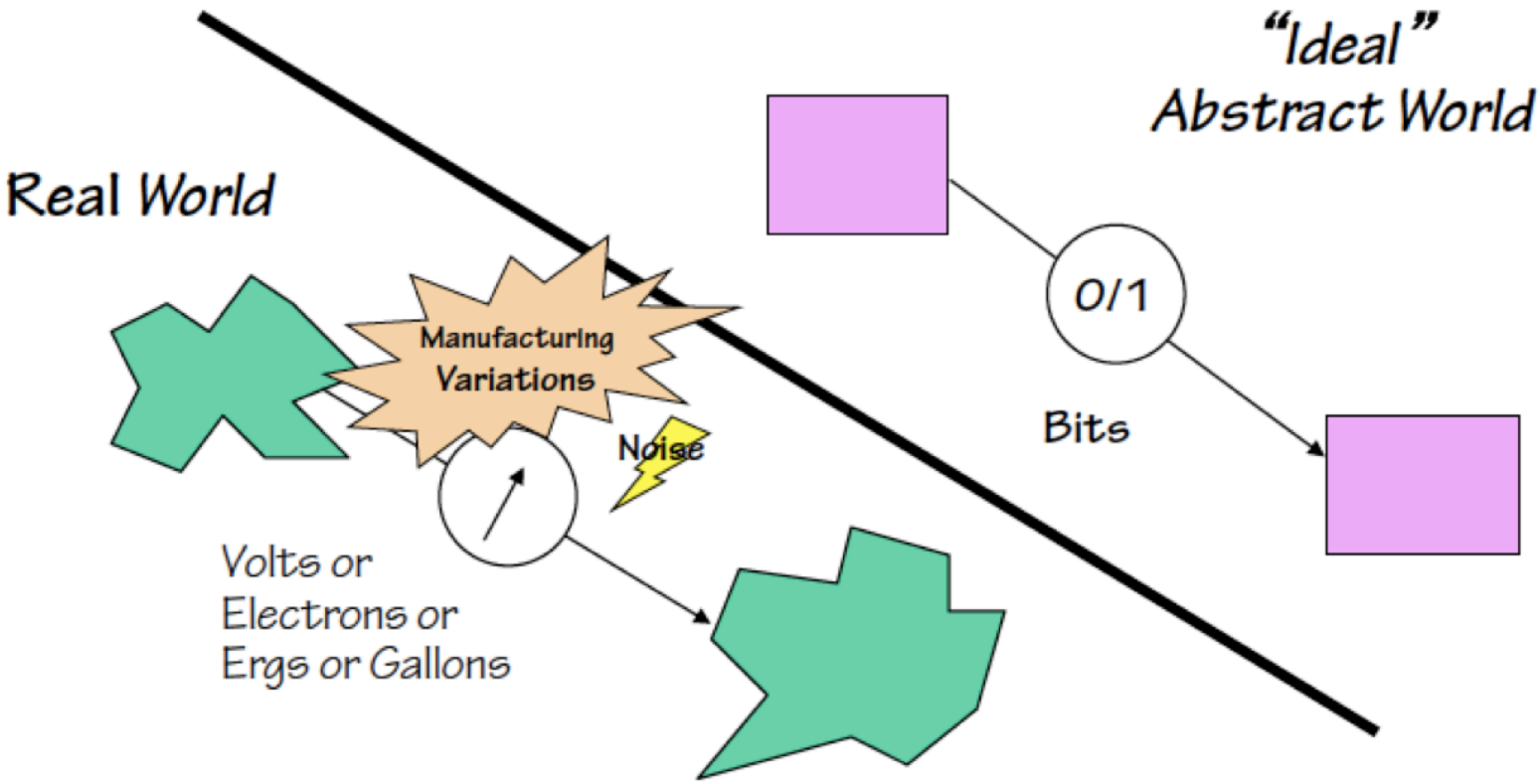
http://www.americanscientist.org/template/AssetDetail/assetid/14340



http://www.digitalphilosophy.org/physicists_model.htm

from Lecture 2 in MIT 6.004 Computation Structures http://6004.csail.mit.edu/

The digital abstraction (II)

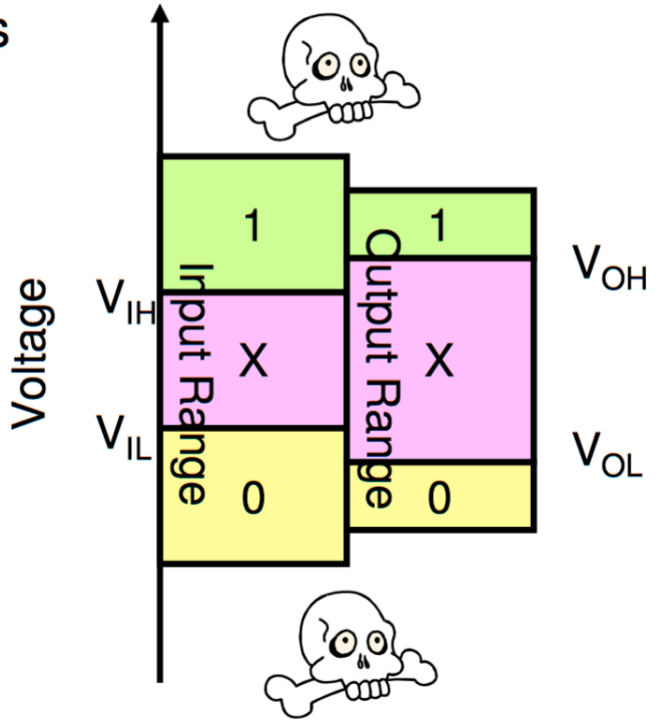


Keep in mind that the world is not digital, we would simply like to engineer it to behave that way. Furthermore, we must use real physical phenomena to implement digital designs!

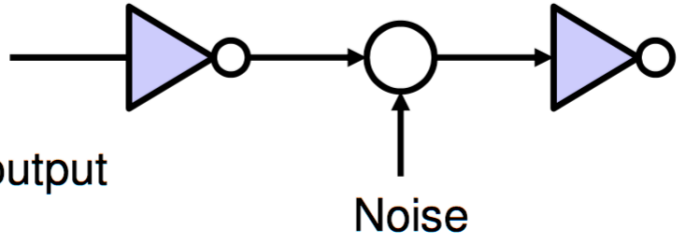
from Lecture 2 in MIT 6.004 Computation Structures http://6004.csail.mit.edu/

The digital abstraction (III)

- Divide voltage into discrete regions
  - Logic 0
  - Logic 1
  - X - between 0 and 1
  - Out of range
    - may damage devices



- Each logic gate *restores* the signal
  - Output noise < input noise
  - Noise is not cumulative
    - In fact it is attenuated
  - Noise margin
    - How much noise won't change output



MOS transistor encoding bits

Rather than worrying about the precise voltages on the terminals of the transistor, guarantee that voltages will fall within two regions, one represents a logic ‘0’ and the other a ‘1’.

Need to compute the output only for inputs in the allowable range

- Much simpler than before
- Model transistor as being either conducting, or off

Need to ensure that the output is always in the allowable voltage range

- Need to make sure you produce valid digital outputs to the next stage
- Also want to have level restore

adapted from Introduction to VLSI Stanford University by Subhasish Mitra

Input-Output voltage ranges and noise

V_{IL}: Maximum input voltage recognized as logic 0

V_{IH}: Minimum input voltage recognized as logic 1

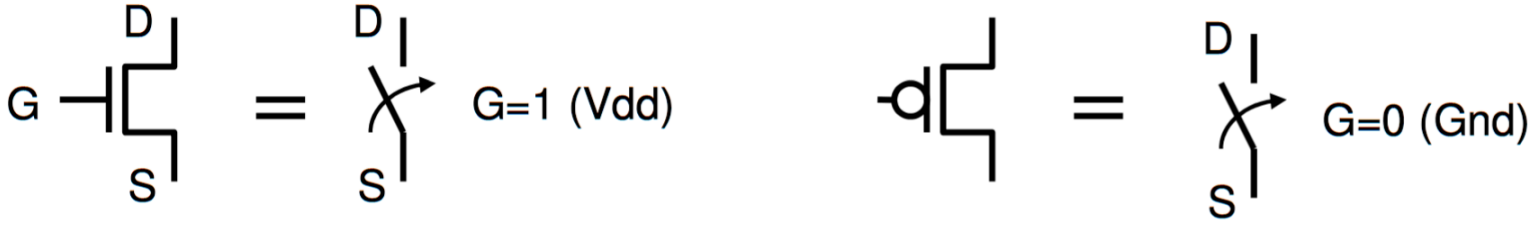
V_{OL}: Maximum output voltage corresponding to logic 0

V_{OH}: Minimum output voltage corresponding to logic 1

- Consider Inverter
  - Suppose Output = V_{OH}
- Suppose this inverter output connected to another inverter input
- If $V_{OH} < V_{IH}$: PROBLEM
  - V_{OH} better be > V_{IH}
- $V_{OH} - V_{IH}$ = NMH (noise margin high)
- NML (Noise margin Low): similar

adapted from Introduction to VLSI Stanford University by Subhasish Mitra

Simplest Model for MOS transistor switch



NMOS transistors PMOS transistors

- Let Logic value 1 be Vdd, value 0 be Gnd
- NMOS devices are switches
  - G is 1 -> the drain D and source S are connected
  - G is 0 -> the drain D and source S are not connected
- PMOS devices are switches
  - G is 0 -> the drain D and source S are connected
  - G is 1 -> the drain D and source S are not connected

adapted from Introduction to VLSI Stanford University by Subhasish Mitra

Terminology

Note that the source and drain terminals are really the same, but by convention the source terminal is the one with the lower voltage on it. Thus, the maximum voltage between the gate and the {source, drain} is the voltage between the source and the gate. (This fact will be important later.)

The voltage on the gate controls the connection between the source and the drain. When the gate is high, the source and drain are connected together. When it is low, the terminals are disconnected.

CAUTION: do NOT use the words “open” and “closed” to describe switches. Is open an open electrical circuit (no flow), or an open fluid valve (flow)? You get opposite results, depending on which analogy you use.

This description is for nMOS transistors. For pMOS everything is reversed. The source is the higher voltage terminal, and the transistor is on when the gate is much lower than the source. More on pMOS later

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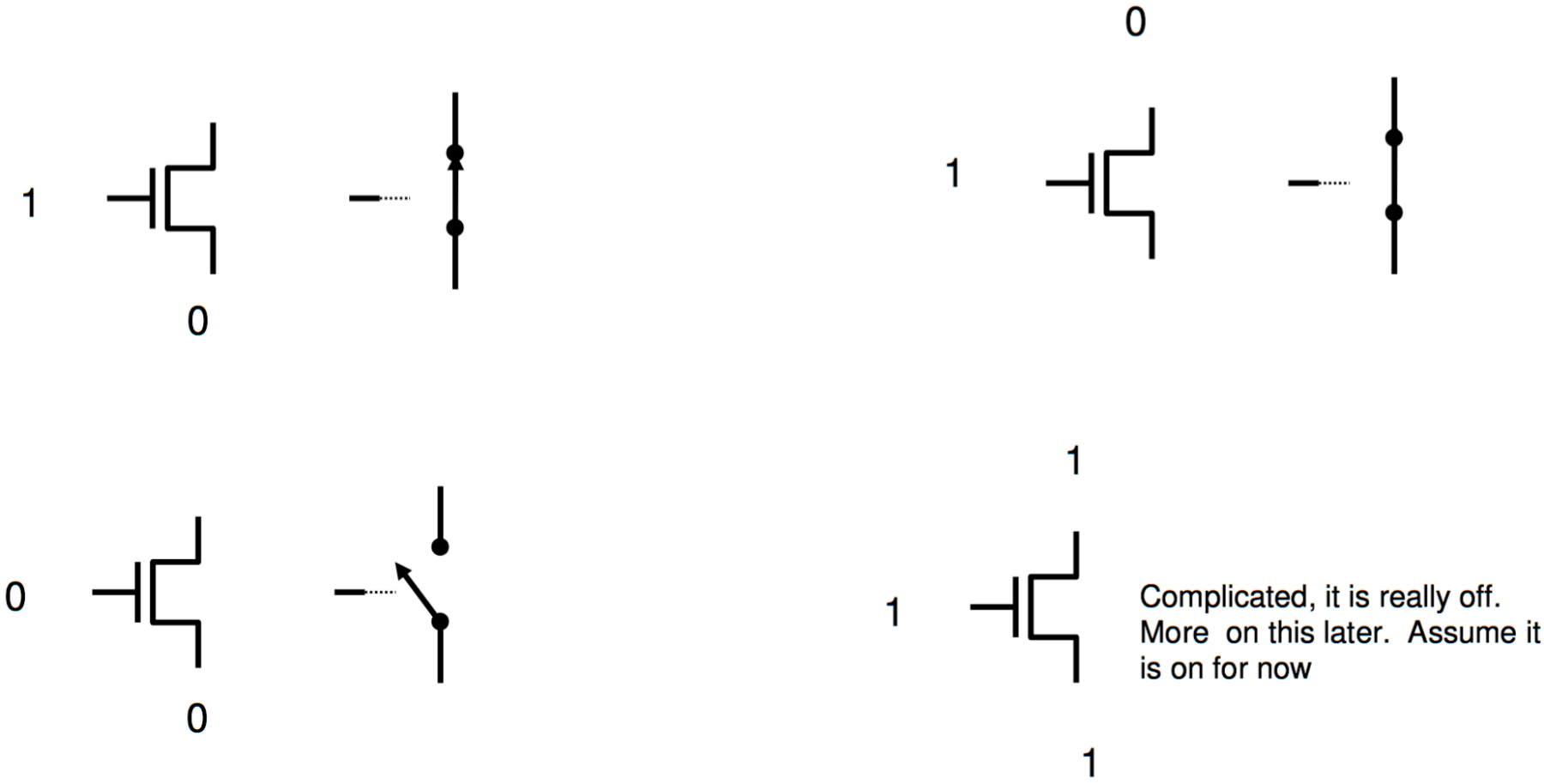
Transistor Examples

The state of these transistors:



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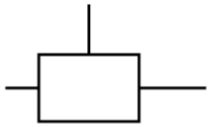
Switch networks (I)

- Since transistors can be modeled as switches
  - Look at what we can make out of switches
  - Draw an abstract switch as



    - Control (gate) terminal is on top
- Can build switch networks
  - Are not logic gates themselves!!!
  - Are a collection of switches that still have two non-control terminals
    - Define function of a switch network as the inputs conditions that connect the two non-control terminals of the network
- Structure of switch network sets its logic functions:
    - 'OR' functions are constructed by parallel switches
    - 'AND' function are constructed by series switches

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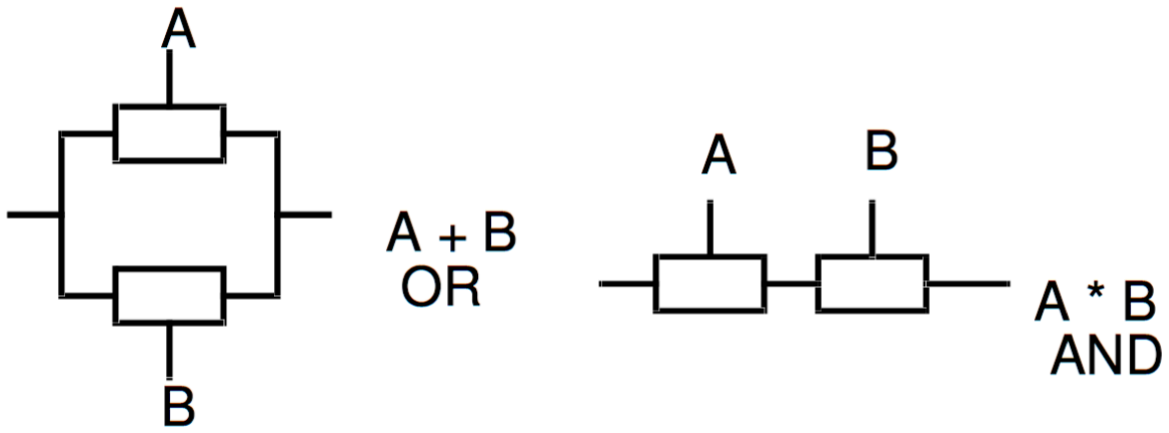
Switch networks (II)



- The function of a switch network is true when the two terminals of the network are connected together. Since for parallel switches the terminals are connected if either switch is on, the function is OR. For series switches the network is conducting only if both switches are on, hence an AND.

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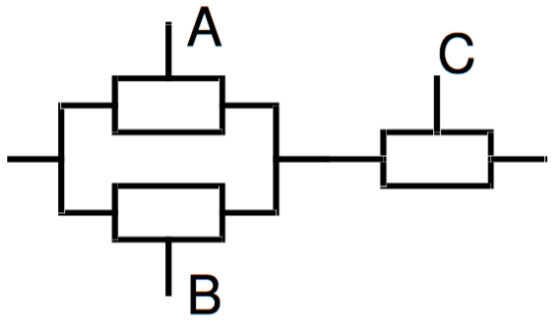
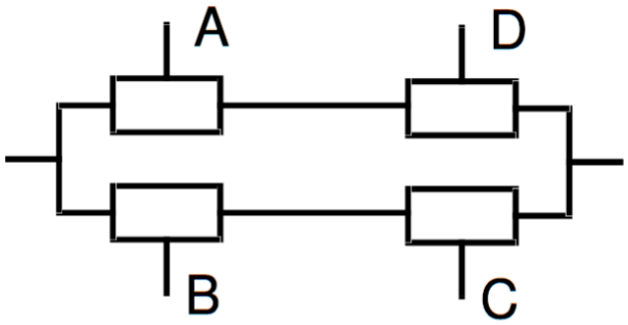
General switch networks



(A + B) C



(AD) + (BC)

- More complex connections are possible
- Composition rules are simple. Use a recursive definition:
  - Parallel combination of switch networks yields an OR of the component switch networks' functions
  - Series combination of switch networks yields on AND of the component switch networks' functions.

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Building functions out of switches

- Have switches, but we want to build logic gate
- Logic gate abstraction:
  - Unidirectional
    - Inputs drive output, but output does not drive inputs
  - Digital gate
    - Reduces input noise
  - Operation completely described by a boolean operator
- Not a difficult task if you follow a few simple rules
  - Connect switches so output is always driven to either Vdd, Gnd
    - Output noise should be small, if power supply noise is small
  - GND and Vdd are never connected to one another
    - Don't want to short the power supply out.

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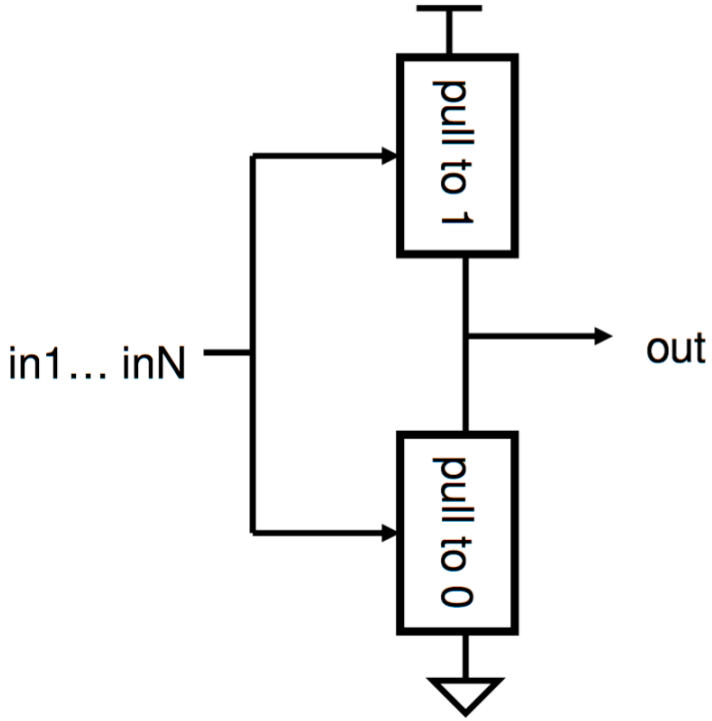
Basic idea: Build two switch networks one good for 1s and one good for 0s



- Requirement 1: output is always driven by one of the two branches
- Requirement 2: output is never driven by both at the same time
- Make the switch functions complementary

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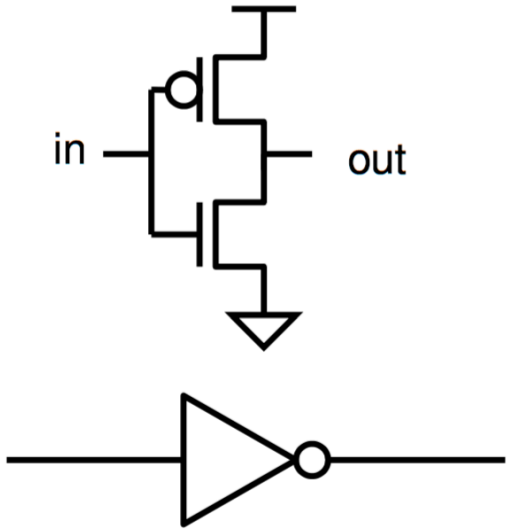
The genesis of the inverter!



- Meets the rules
  - Out is always driven (Either pMOS or nMOS is always active)
  - Vdd and Gnd are never shorted
    - At least with valid inputs

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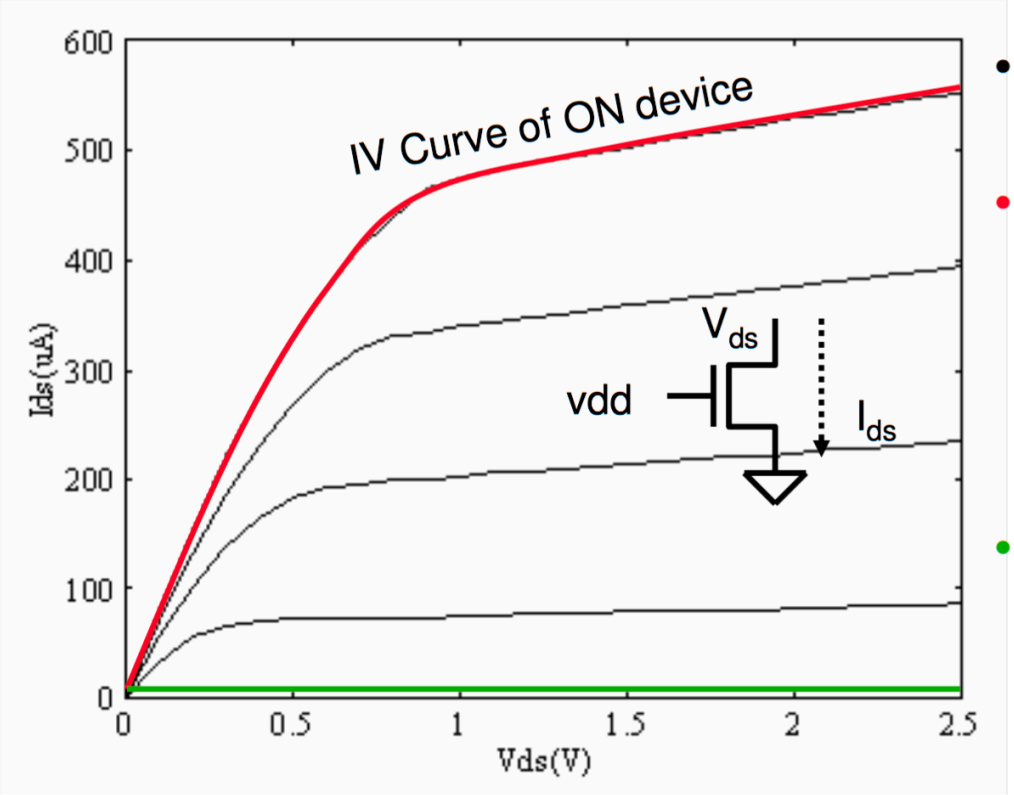
More gates next lecture!

NMOS is good for "transmitting" 0s:
because current from Drain to Source pulls low



- Operates on one of two curves
- on
  - Looks like a current source initially (high V_{ds})
  - Looks like a resistor later (low V_{ds})
- off
  - Open circuit always

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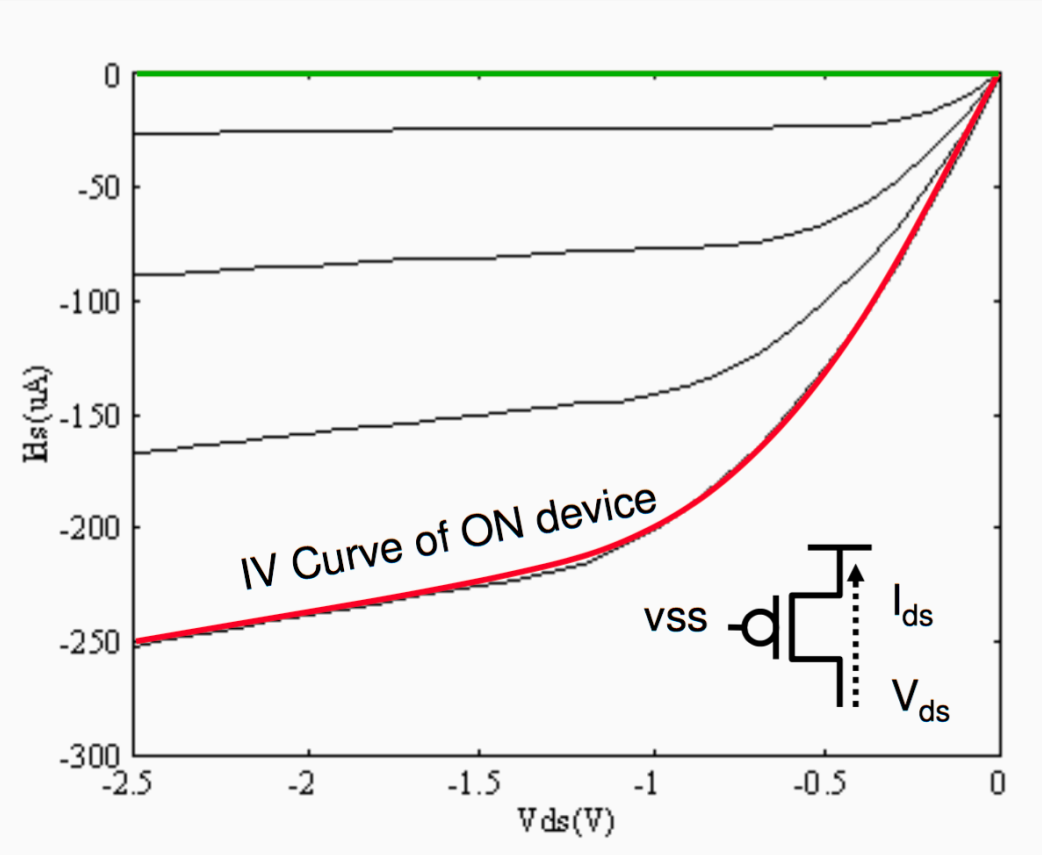
PMOS is good for "transmitting" 1s:
because current from Drain to Source pulls high



- Same behavior as NMOS
  - Open circuit when off
  - Current source or resistor when on

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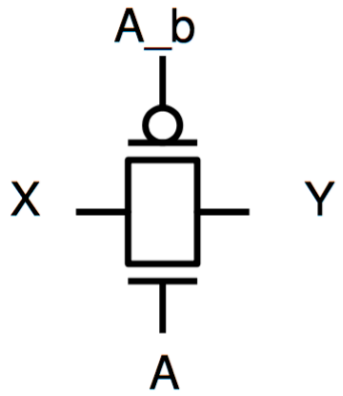
CMOS pass transistor structures



- Concept of switch is really versatile
  - But if we don't know the value being switched, neither NMOS nor PMOS alone implements it
- Solution: use nMOS and pMOS in parallel
  - Drive gates with complementary signals
  - Completely bidirectional
- How can we take advantage of this?

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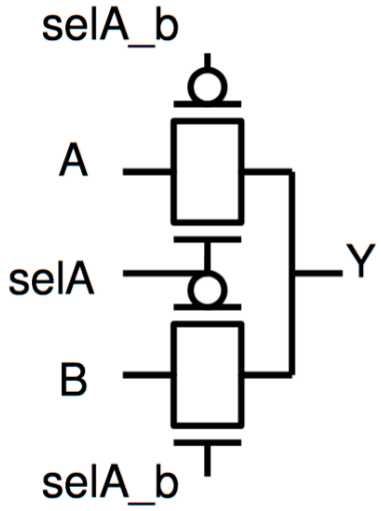
Transmission gate muxes



- Arbitrary number of inputs can be muxed together
  - As long as selects are mutually exclusive
- Can be cascaded in series to make more complicated networks
- CAREFUL: Not restoring as drawn (no gain)
  - Inverter often used to buffer output
- More on using transmission gates later

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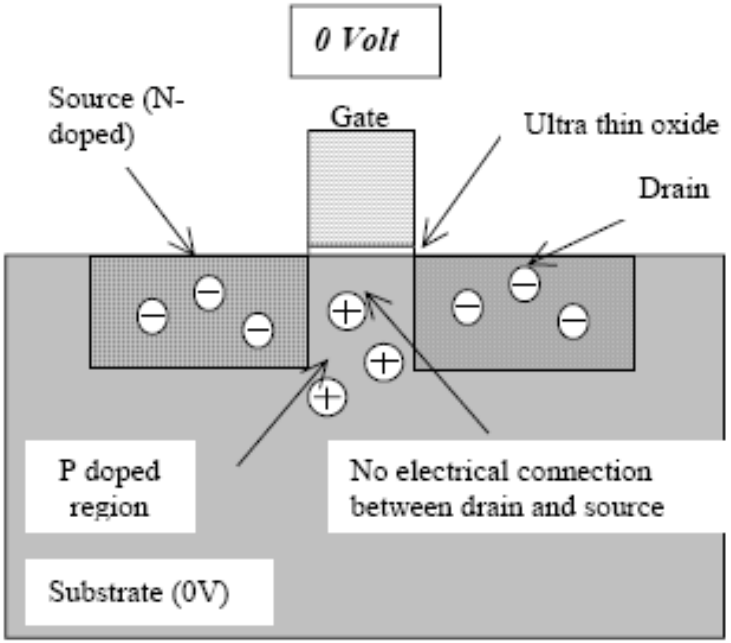
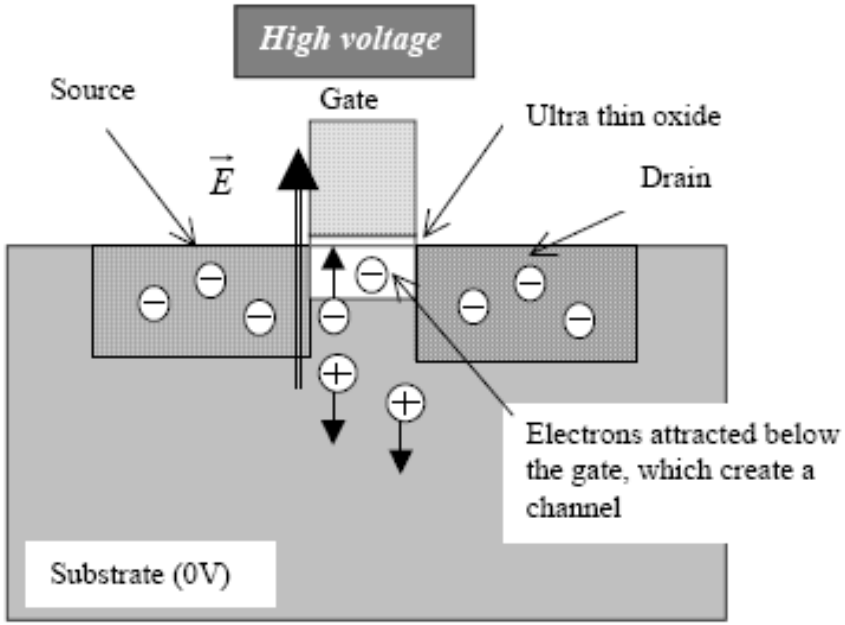
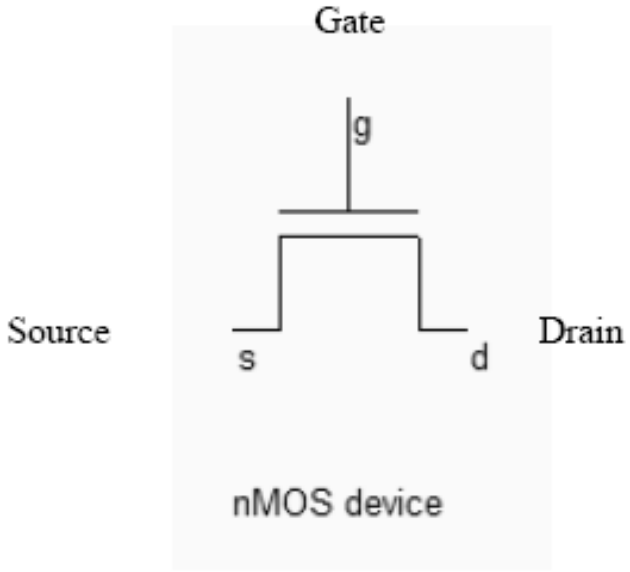
logic levels definitions

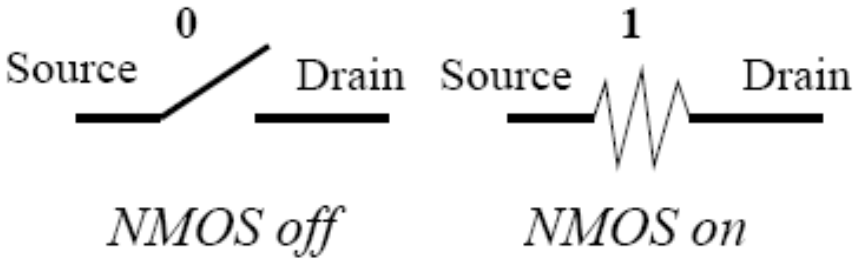
Logical value	Voltage	Name	Symbol in DSCH	Symbol in Microwind
0	0.0V	VSS	 (Green in logic simulation)	 (Green in analog simulation)
1	1.2V in cmos 0.12µm	VDD	 (Red in logic simulation)	 (Red in analog simulation)
X	Undefined	X	(Gray in simulation)	(Gray in simulation)

MOS transistor

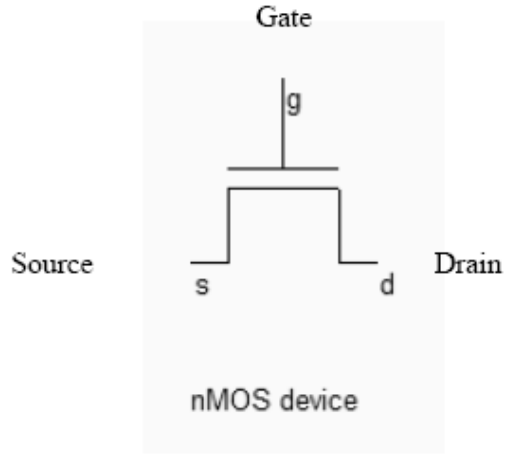




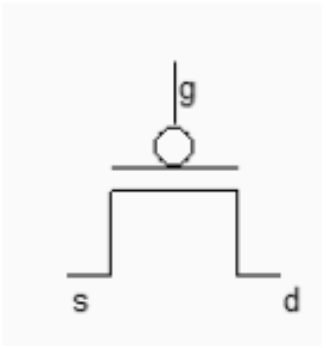


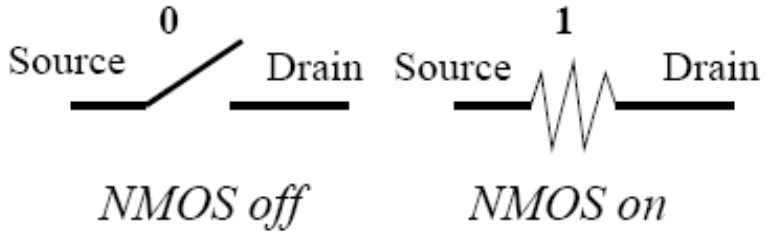


NMOS and PMOS digital "models"

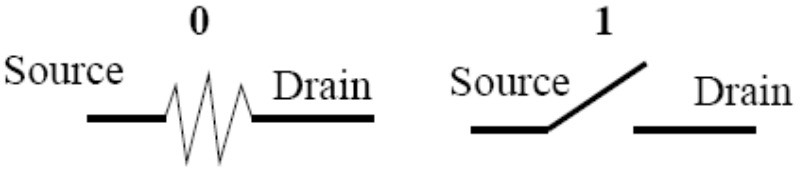


pMOS





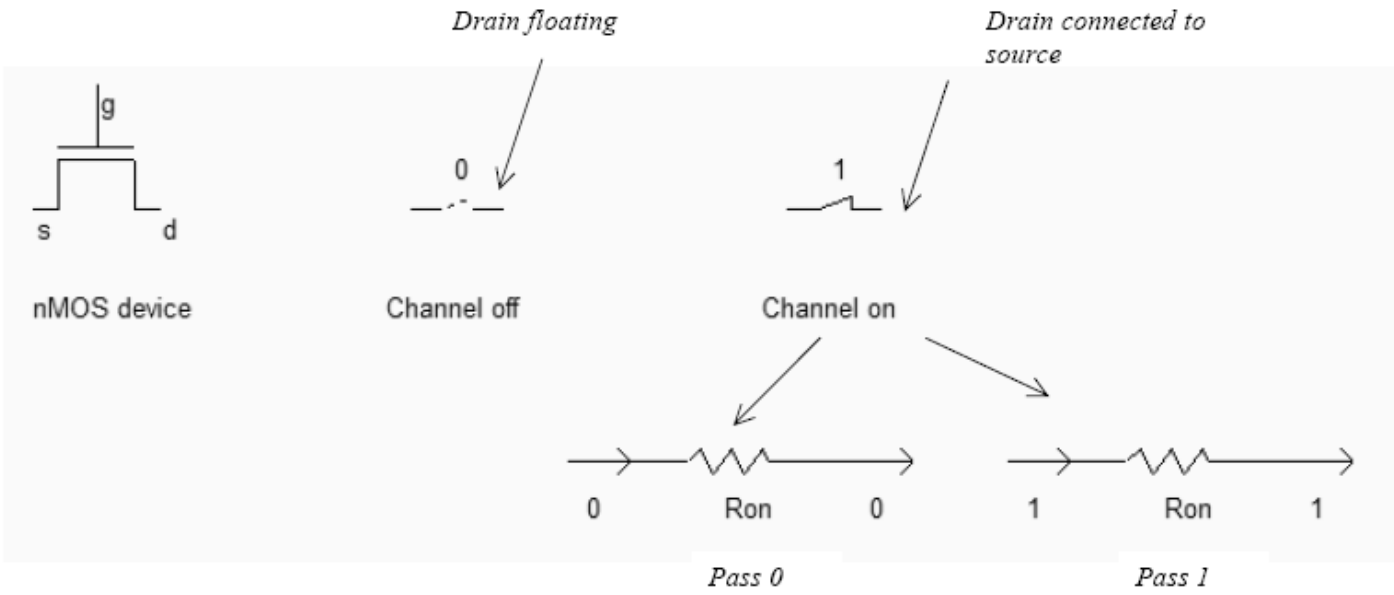
NMOS off *NMOS on*

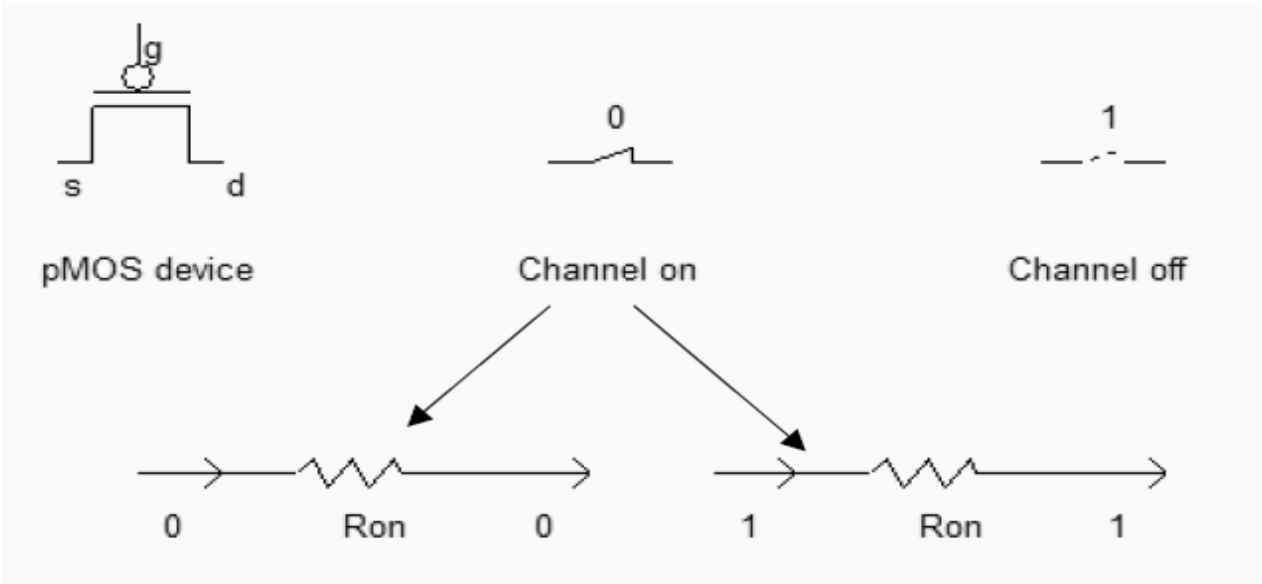


Gate	Source	Drain
0	0	X
0	1	X
1	0	0
1	1	1

Gate	Source	Drain
0	0	0
0	1	1
1	0	X
1	1	X

what does this all mean?

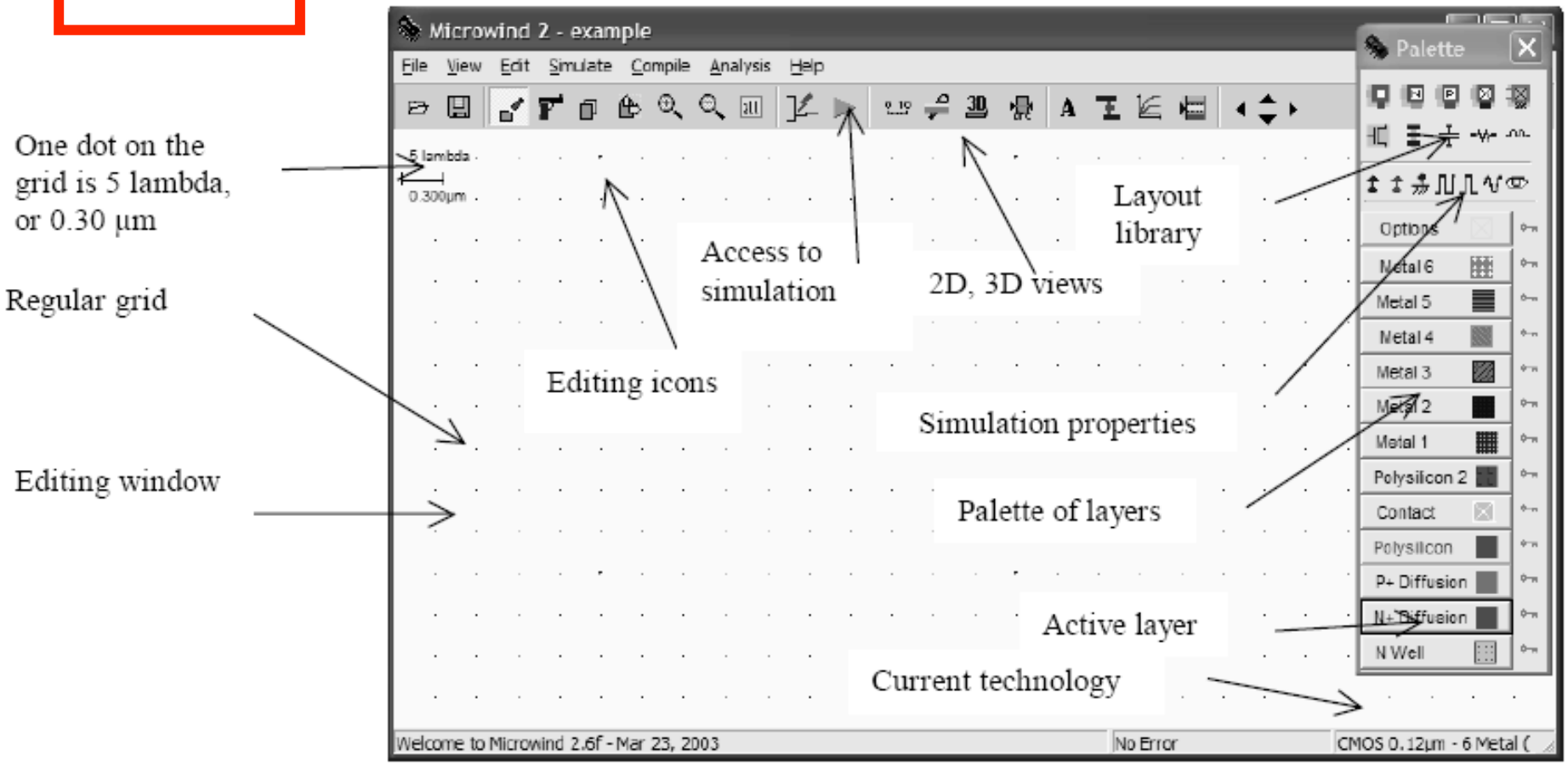




microwind

$$\lambda = \frac{L_{min}}{2}$$

0.12 um CMOS process



and back to layout

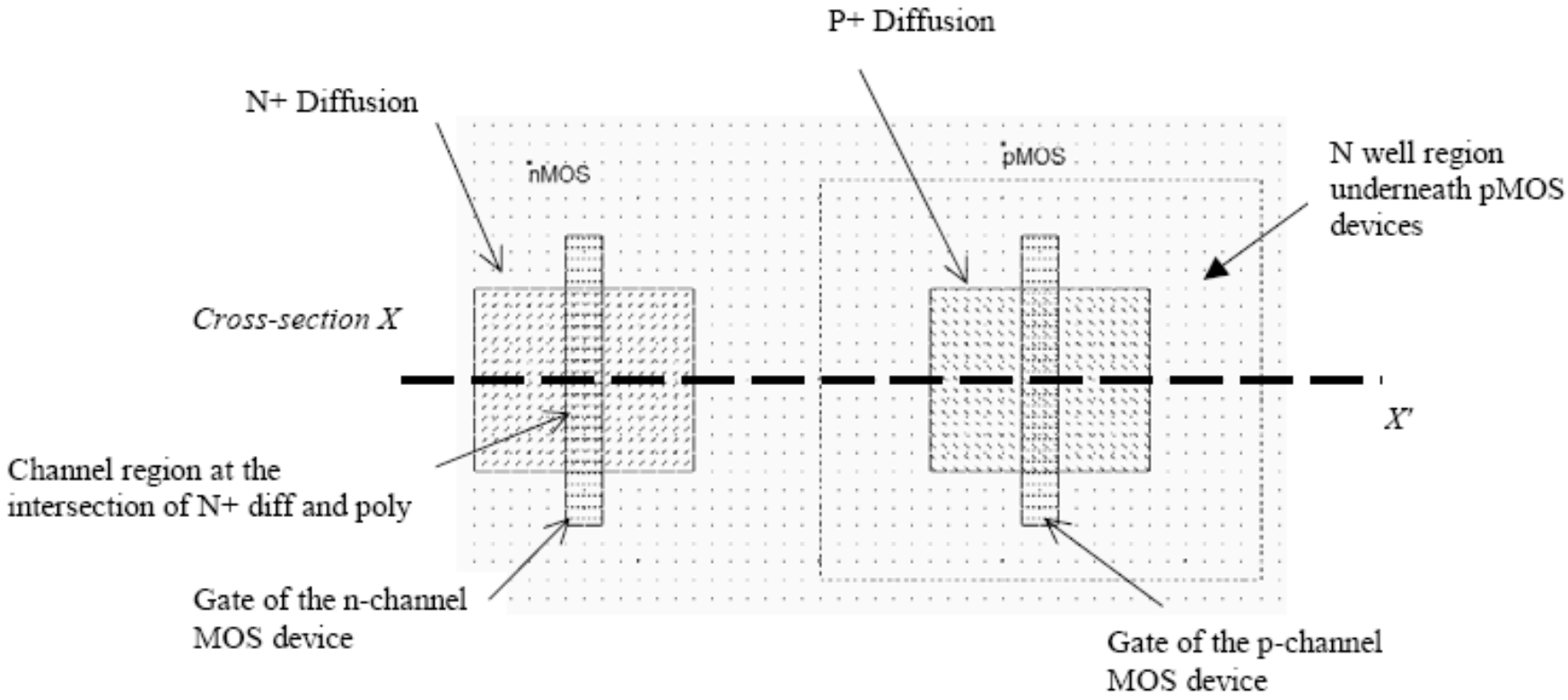


Figure 2-14: Bird's view of the n-channel and p-channel MOS device layout (allMosDevices.MSK)

cross-section and zoom

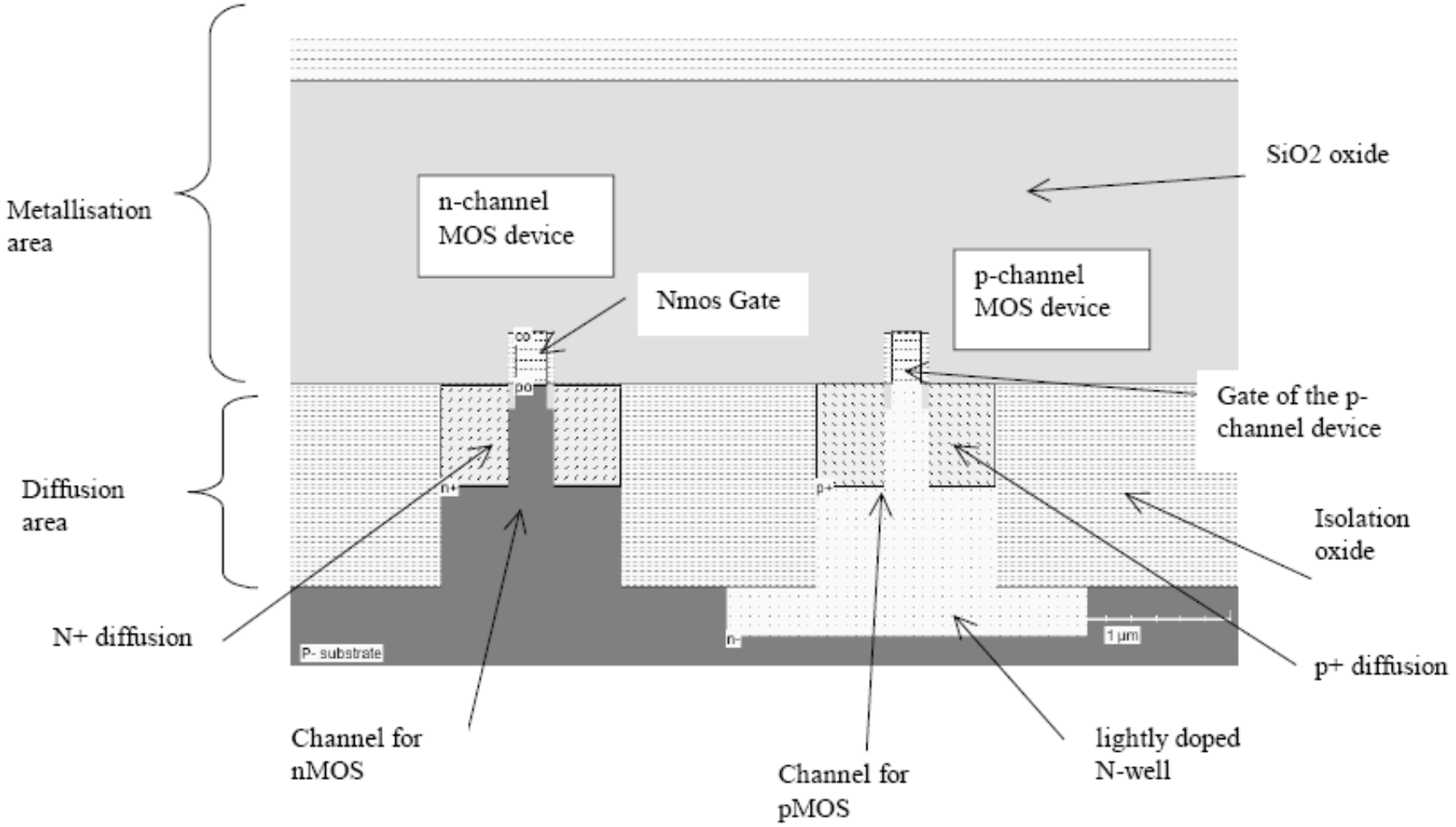
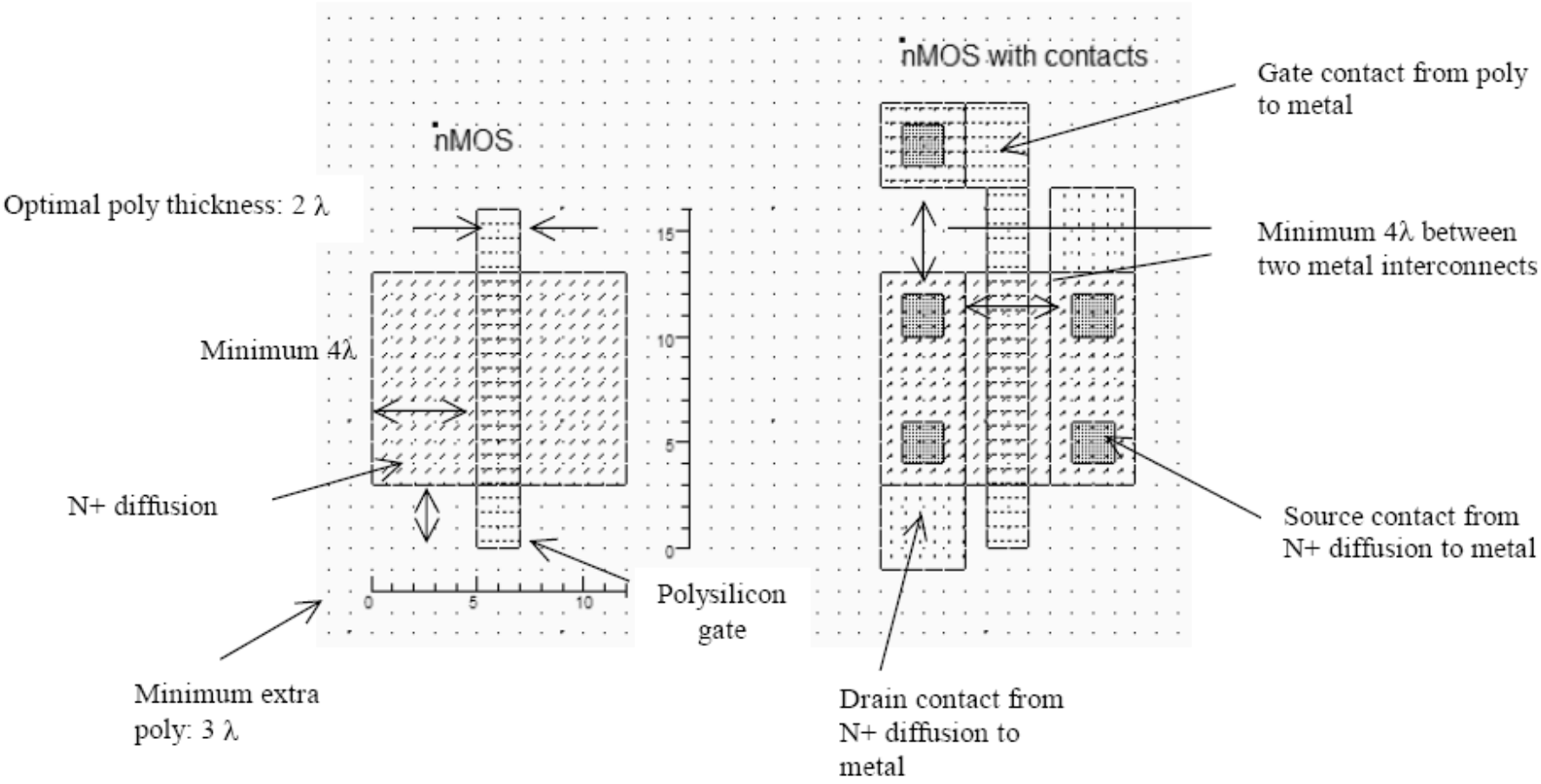


Figure 2-15: Vertical cross-section of an n-channel and p-channel MOS devices in 0.12µm technology

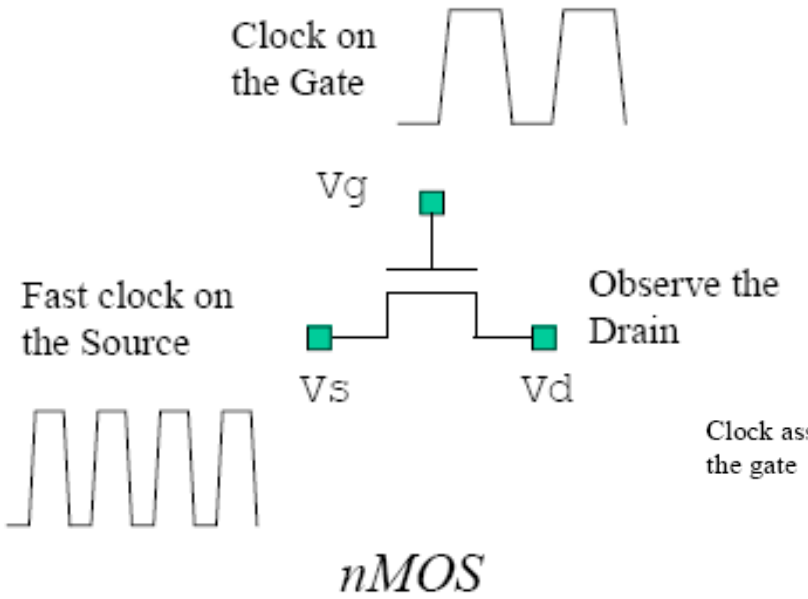
MOS transistor layout

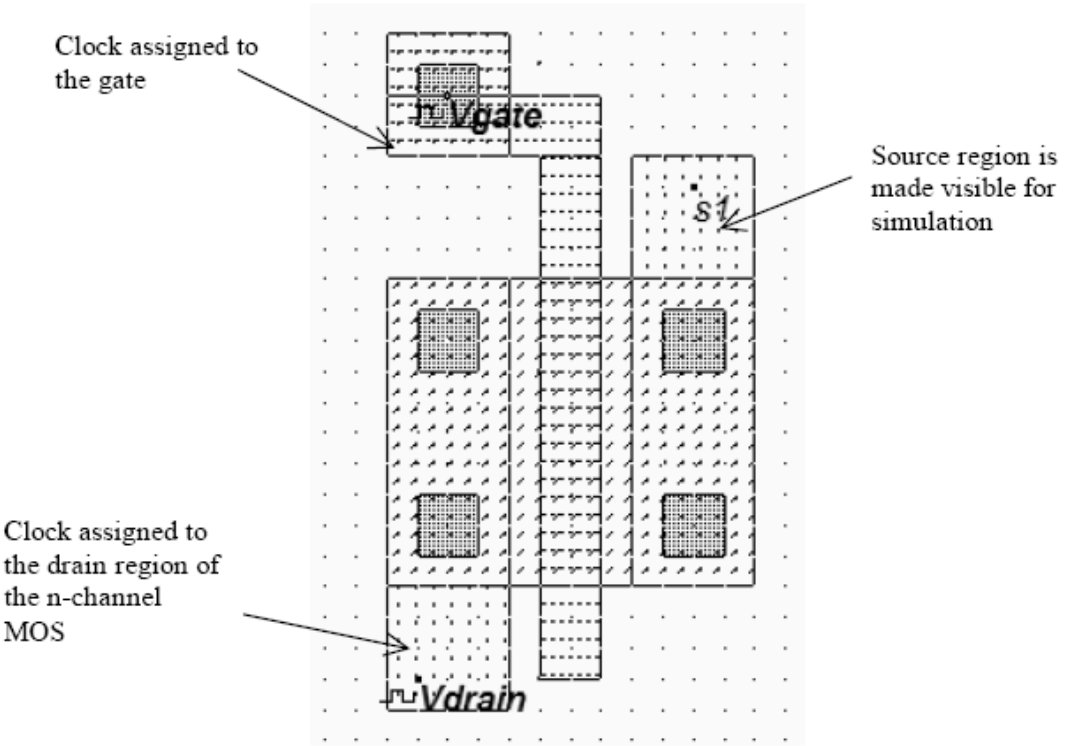


more notation

Layer name	Code	Description	Color in Microwind
Polysilicon	Poly	Gate of the n-channel and p-channel MOS devices	Red
N+ diffusion	Diffn	Delimits the active part of the n-channel device. Also used to polarize the N-well	Dark green
P+ diffusion	Diffn	Delimits the active part of the p-channel device. Also used to polarize the bulk	Maroon
Contact	Contact	Makes the connection between diffusions and metal for routing. The contact plug is fabricated by drilling a hole in the oxide and filling the hole with metal.	White cross
First level of metal	Metal1	Used to rout devices together, in order to create the logic or analog function	Blue
N well	Nwell	Low doped diffusion used to invert the doping of the substrate. All p-channel MOS are located within N well areas.	Dotted green

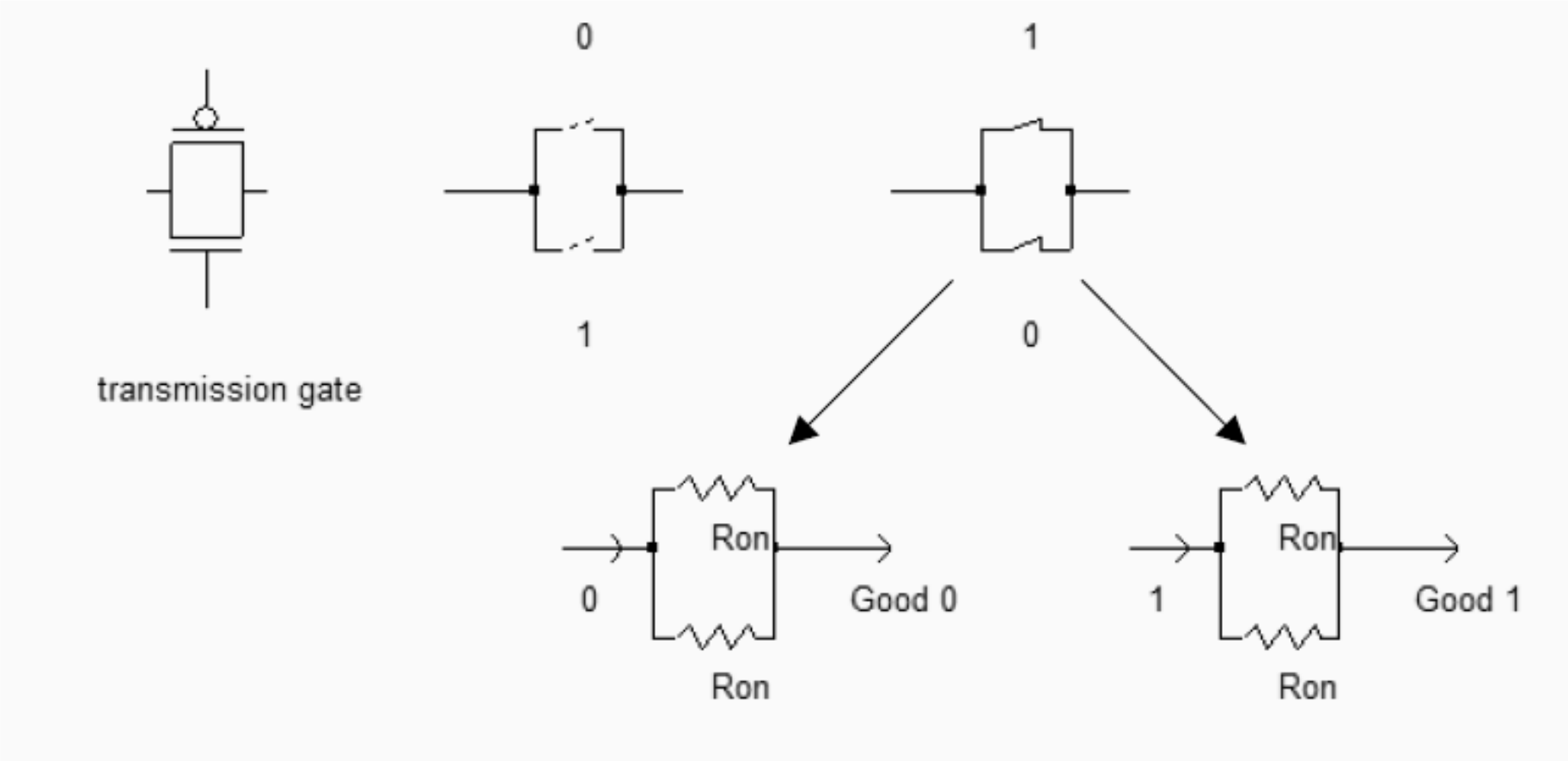
dynamic behavior: another level of abstraction



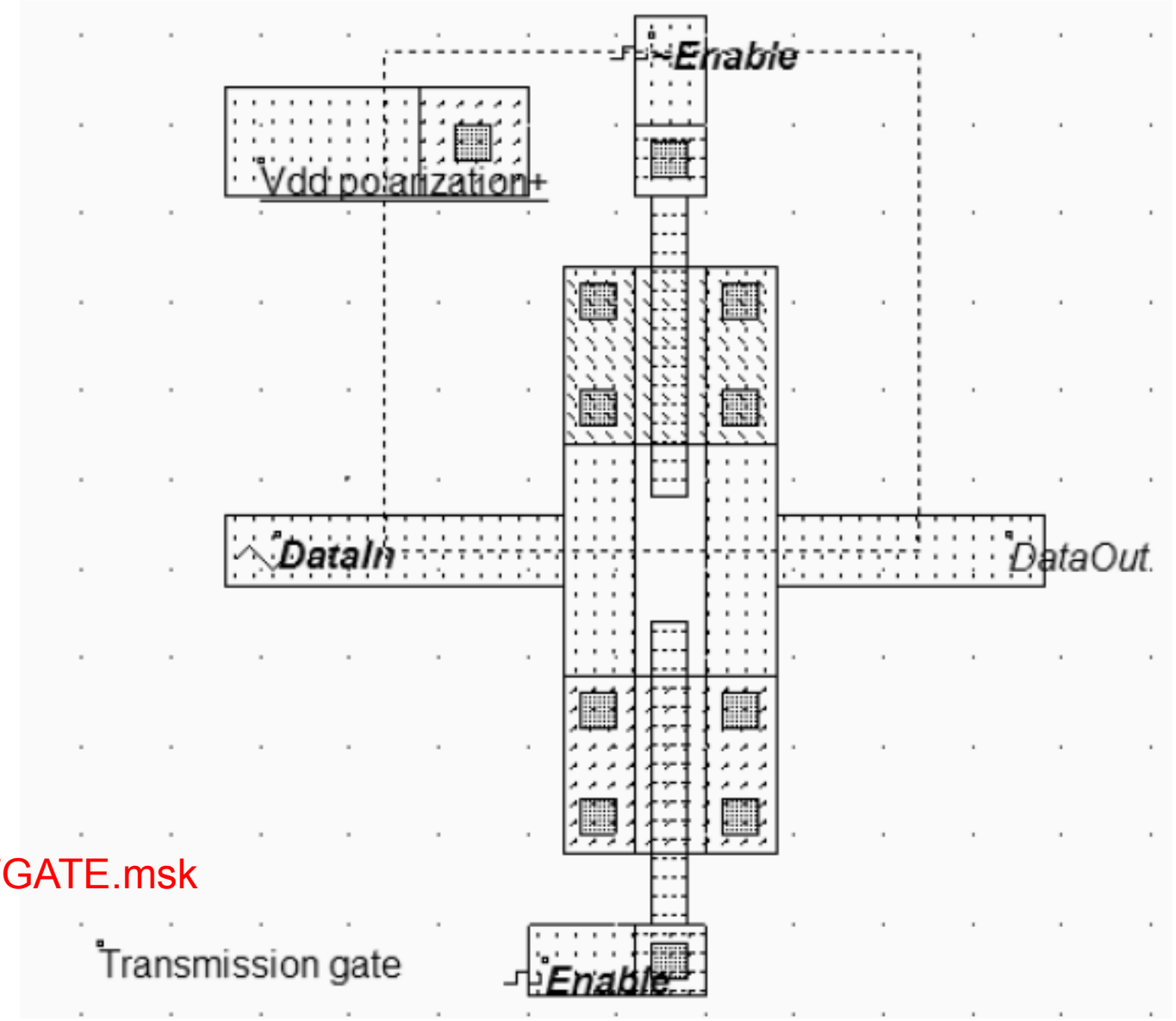


Demo: MOSN.msk

and the perfect switch!



simulation of the perfect switch



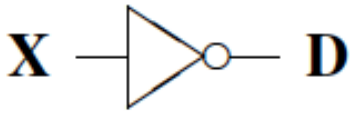
Demo: TGATE.msk

CMOS Inverter

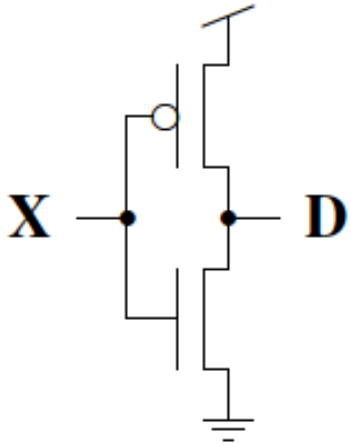
- NFET's pull down, PFET's pull up
- Pull up and pull down NOT at the same time
- Output always connected to VDD or GND

X	D
0	1
1	0

(a)



(b)



(c)

$\mathbf{D = \overline{X}}$

(d)

multiple contacts: why?

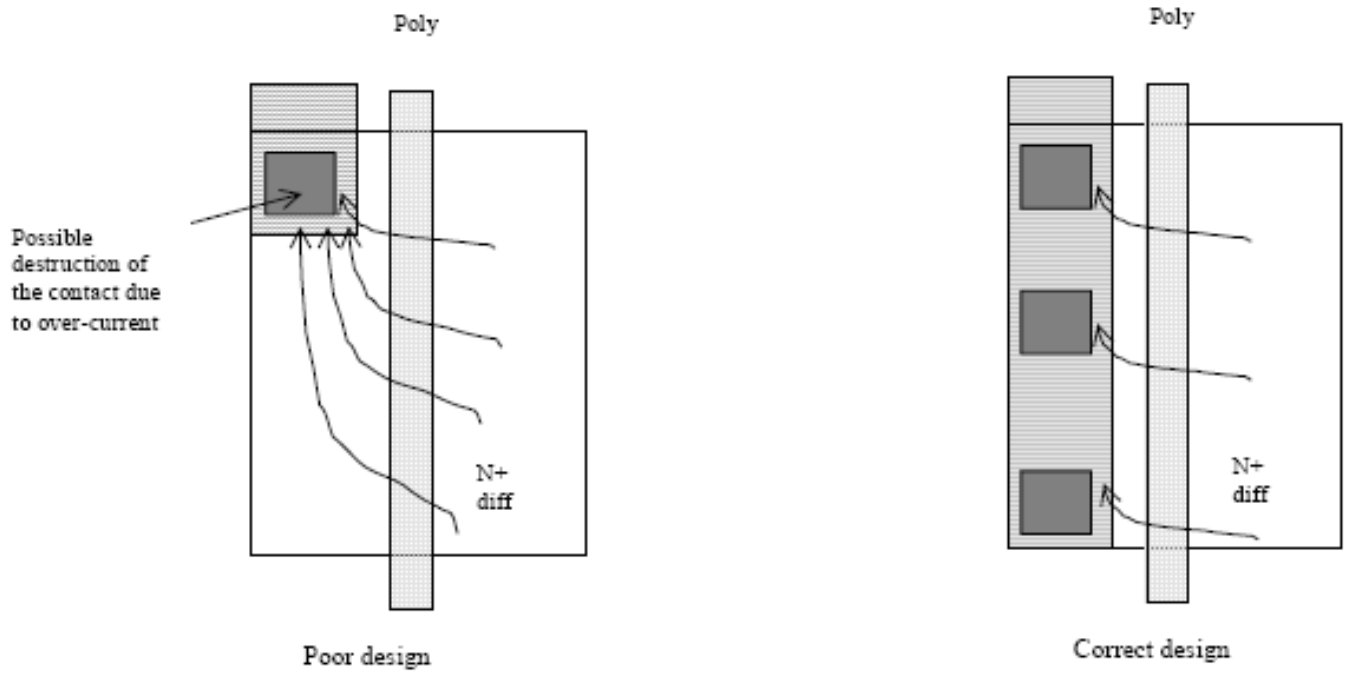


Fig.2-46. A strong current through a single contact could damage the metal structure.

multiple contacts

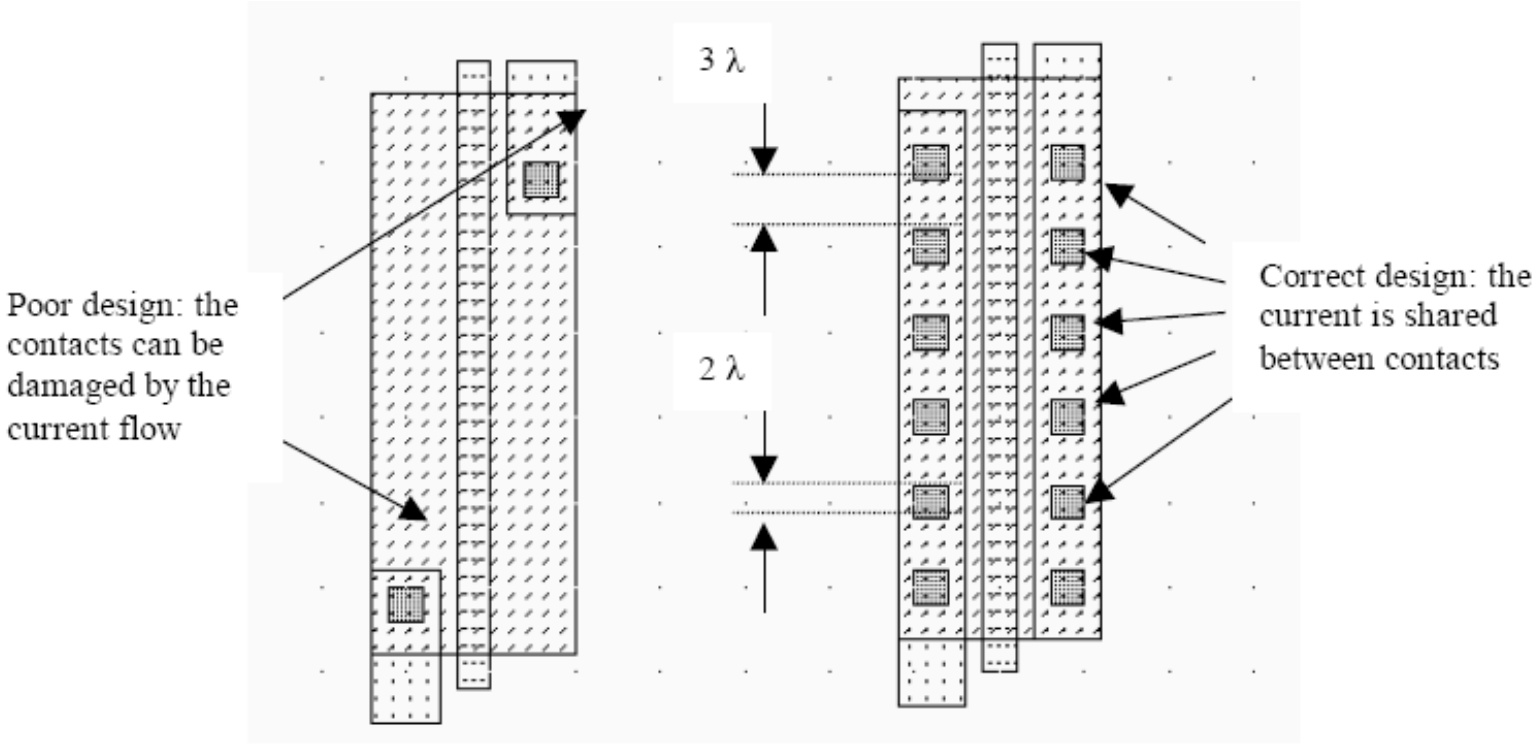


Fig.2-47. A single contact cannot handle more that 1mA. A series of contacts is preferred (MosLayout.MSK)

multiple contacts

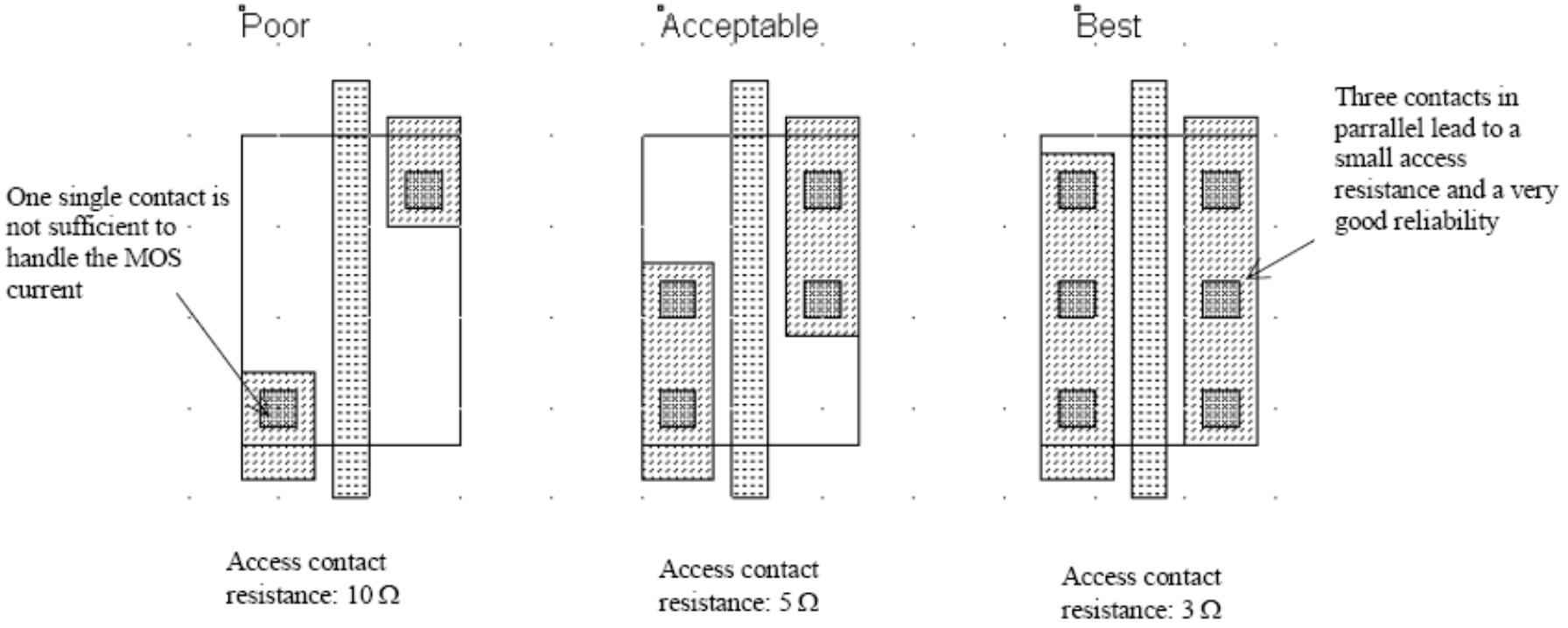


Fig.2-48. A series of contacts also reduced the serial access resistance(MosContacts.MSK)

Computer Aided Design Tools