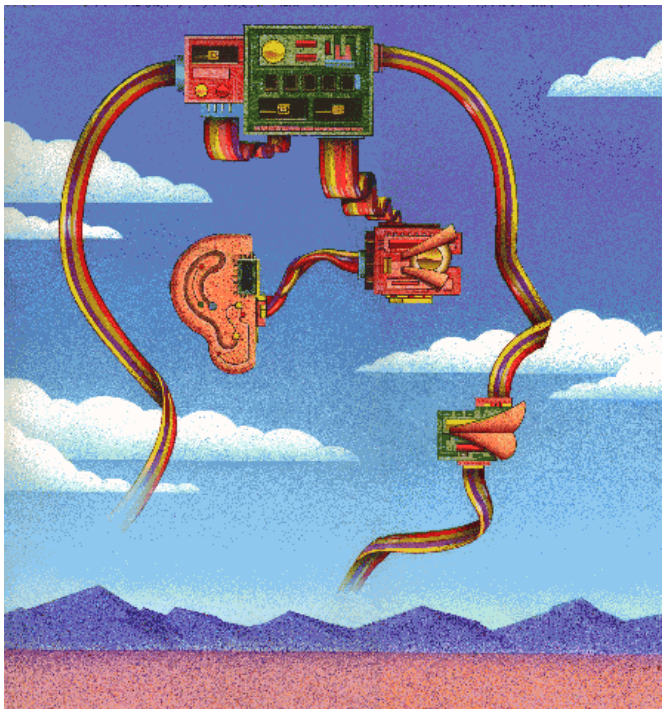
Complex CMOS Gates



Andreas G. Andreou
Pedro Julian

Electrical and Computer Engineering
Johns Hopkins University

http://andreoulab.net

Levels of Abstraction –MOS switch and Inverter-

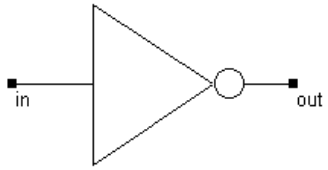
Out = NOT (In)

Out = ~ (In)

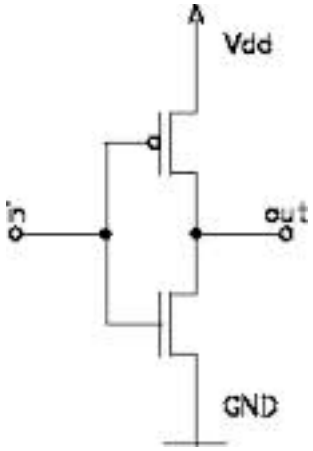
Equation

In	Out
0	1
1	0
X	X

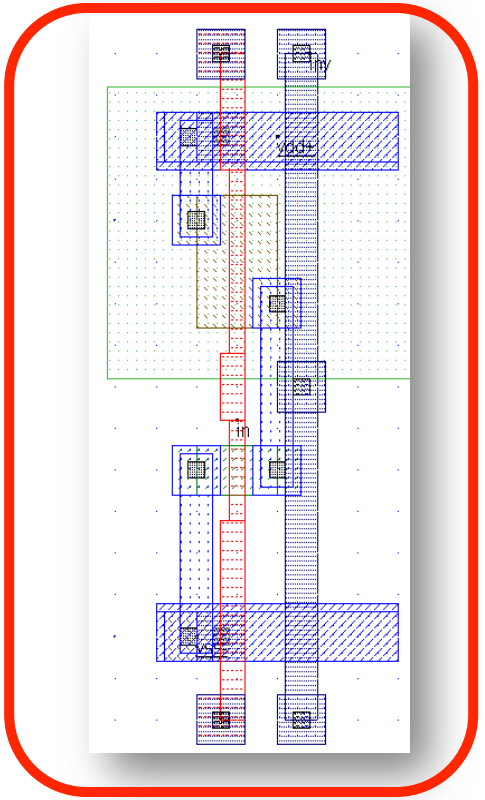
Truth Table



Symbol

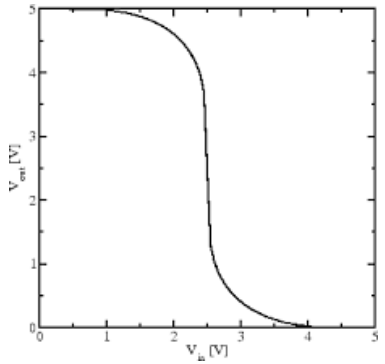


Circuit



Layout

Voltage Transfer Characteristics (VTC)



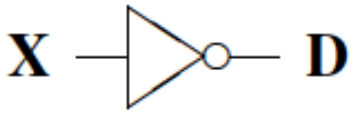
LOGICAL PHYSICAL

Important rules

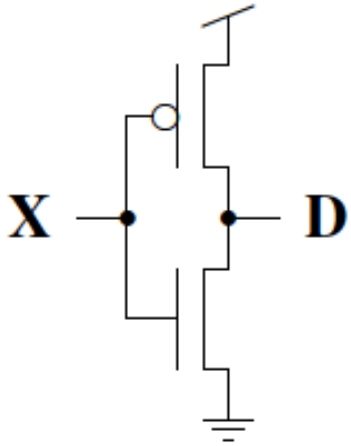
- NFET's pull down, PFET's pull up
- Pull up and pull down NOT at the same time
- Output always connected to VDD or GND

X	D
0	1
1	0

(a)



(b)



(c)

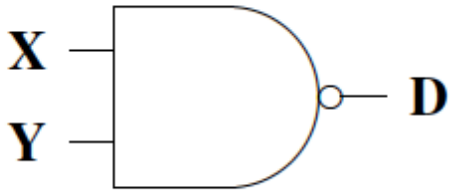
$\mathbf{D = \overline{X}}$

(d)

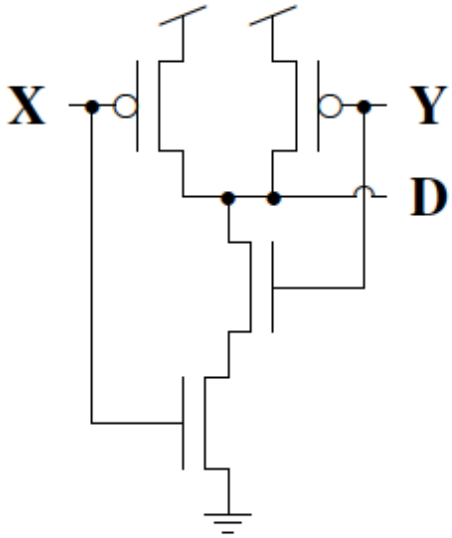
NAND Gate

Y	X	D
0	0	1
0	1	1
1	0	1
1	1	0

(a)



(b)

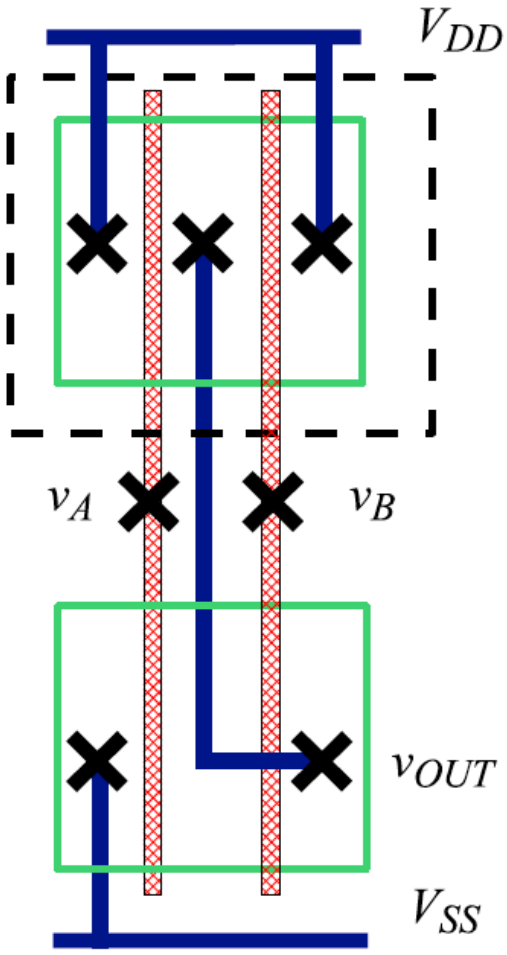


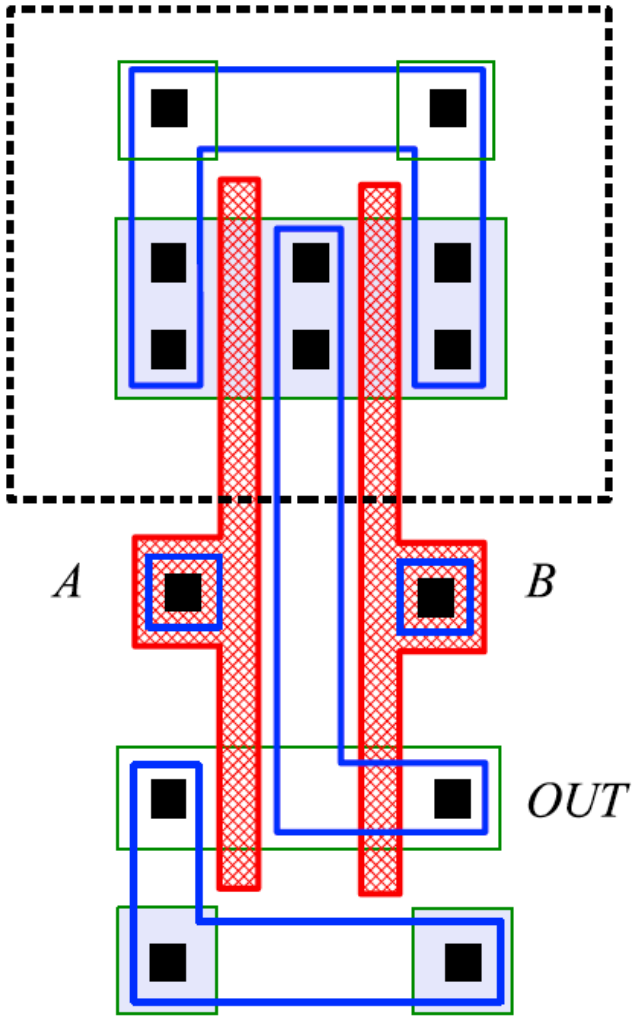
(c)

$$D = \overline{X \cdot Y}$$

(d)

NAND2



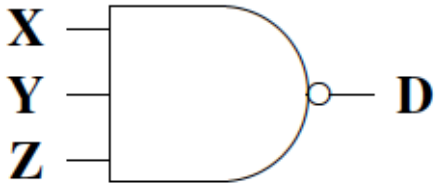


NAND Gate

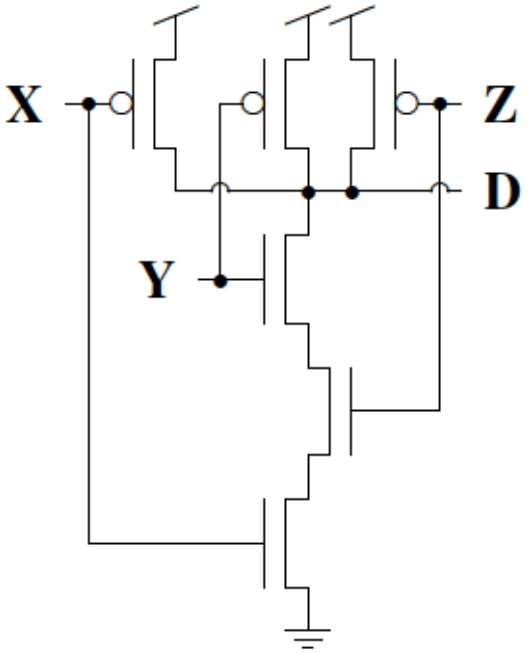
- Three inputs

Z	Y	X	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(a)



(b)



(c)

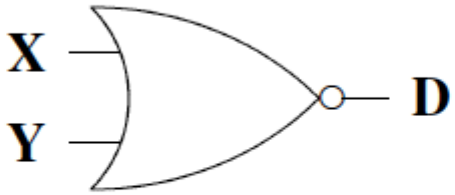
$$D = \overline{X \cdot Y \cdot Z}$$

(d)

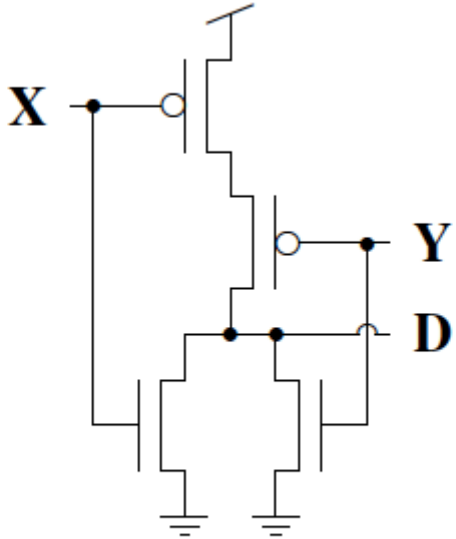
NOR Gate

Y	X	D
0	0	1
0	1	0
1	0	0
1	1	0

(a)



(b)

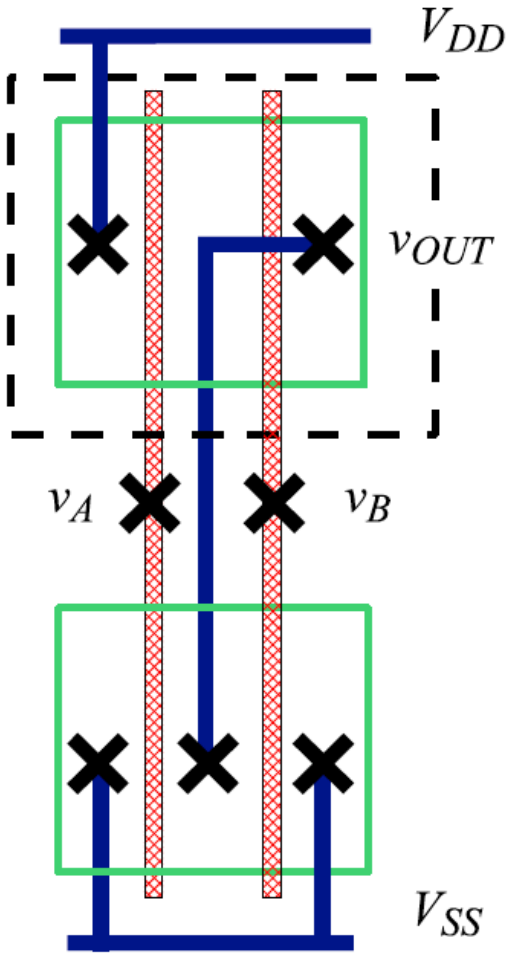


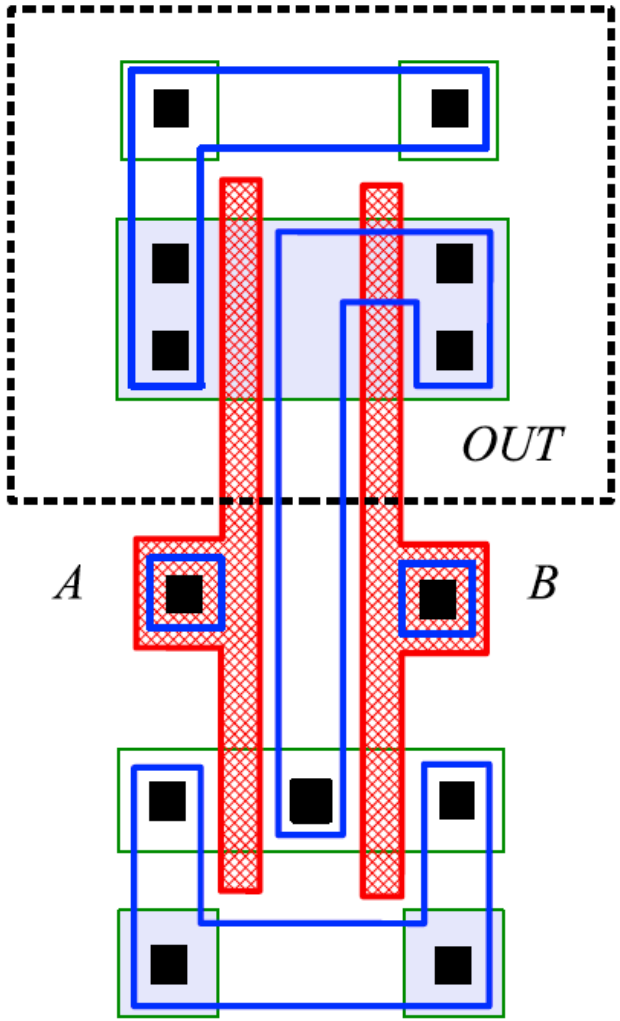
(c)

$$\mathbf{D} = \overline{\mathbf{X} + \mathbf{Y}}$$

(d)

NOR2

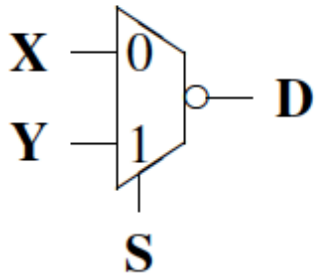




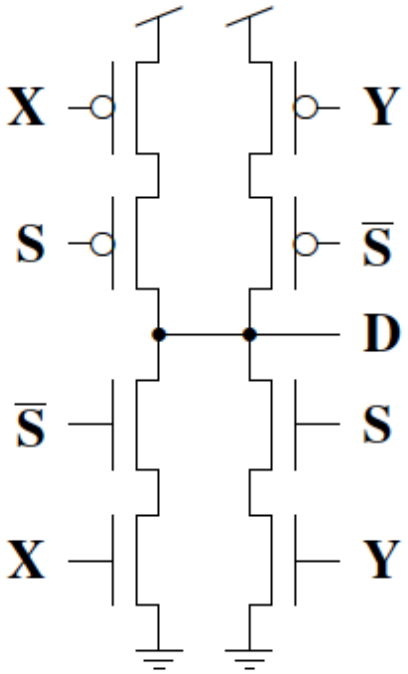
Multiplexer

S	Y	X	D
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(a)



(b)



(c)

$$D = \overline{X \cdot \overline{S} + Y \cdot S}$$

(d)

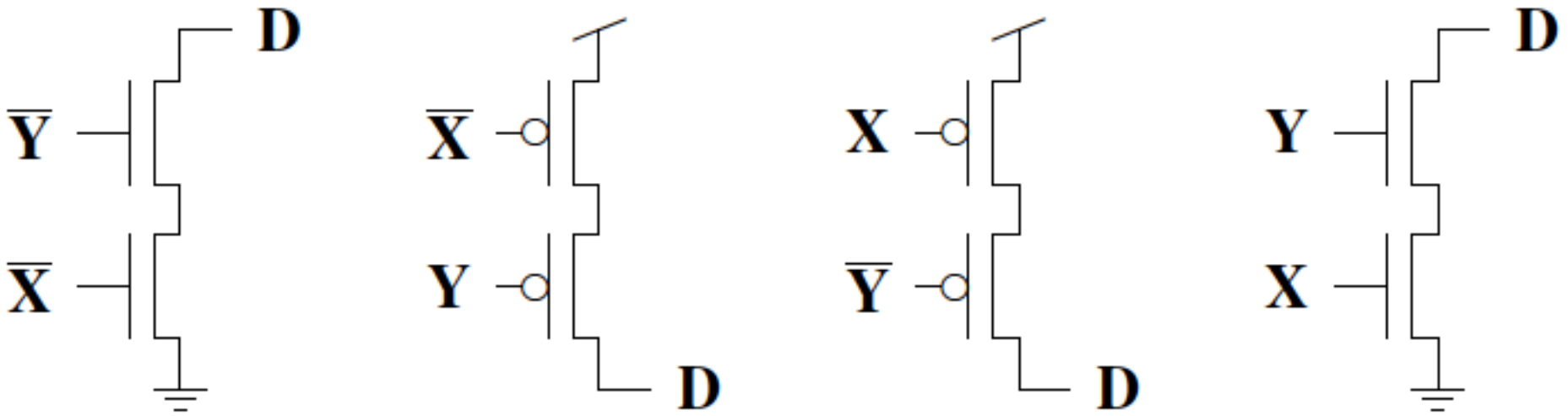
Gate Construction

- Truth table method
- Complementary structures

Truth table method

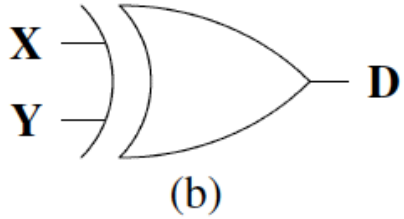
- Example

Y	X	D	
0	0	0	Line 0
0	1	1	Line 1
1	0	1	Line 2
1	1	0	Line 3

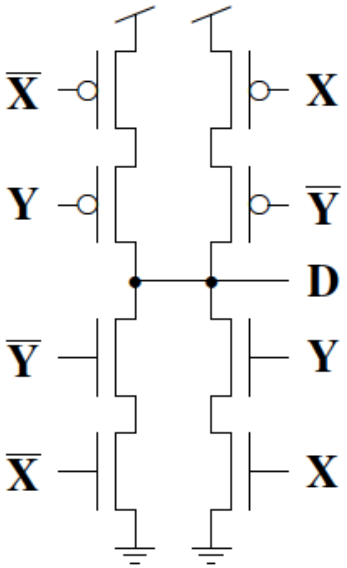


Truth table method

- Result



(b)



(c)

$D = X \oplus Y$
(d)

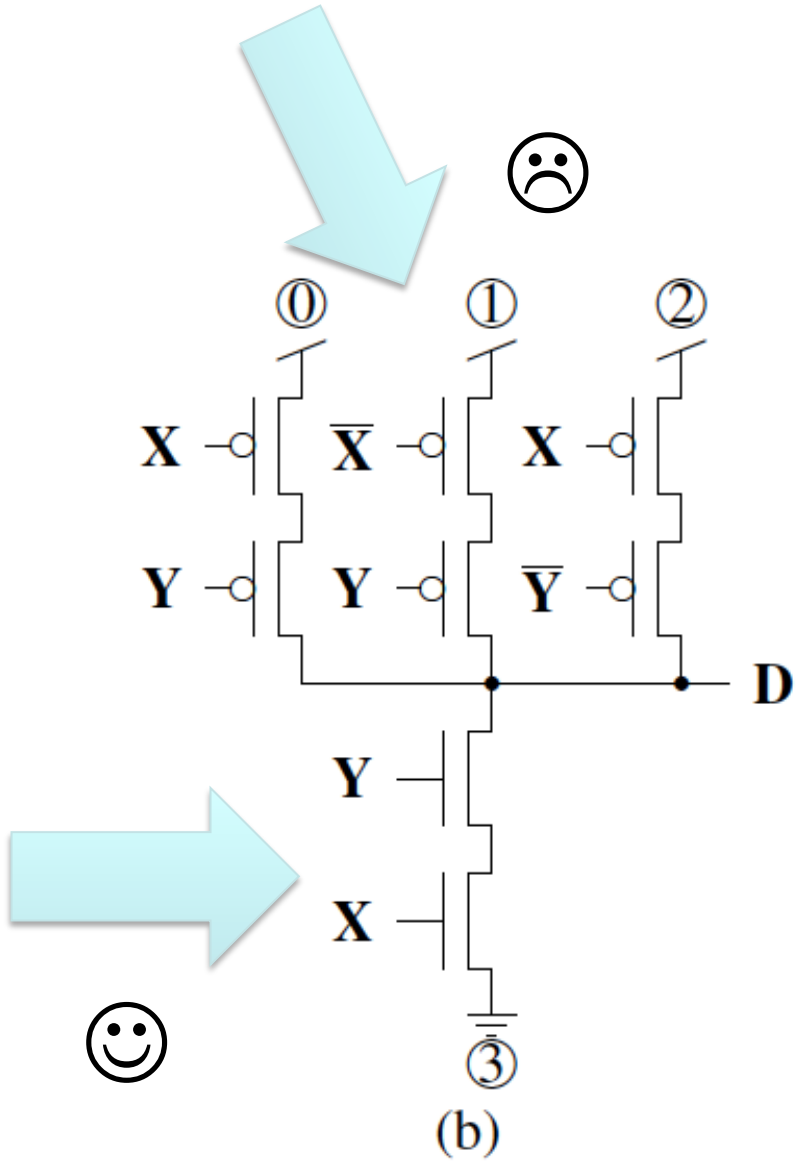
- Disadvantage: n inputs -> 2^n entries. 2^n x n FETs
- We need inverters to generate $\overline{x}$ and $\overline{y}$

Truth table method

- NAND gate

Y	X	D	
0	0	1	Line 0
0	1	1	Line 1
1	0	1	Line 2
1	1	0	Line 3

(a)



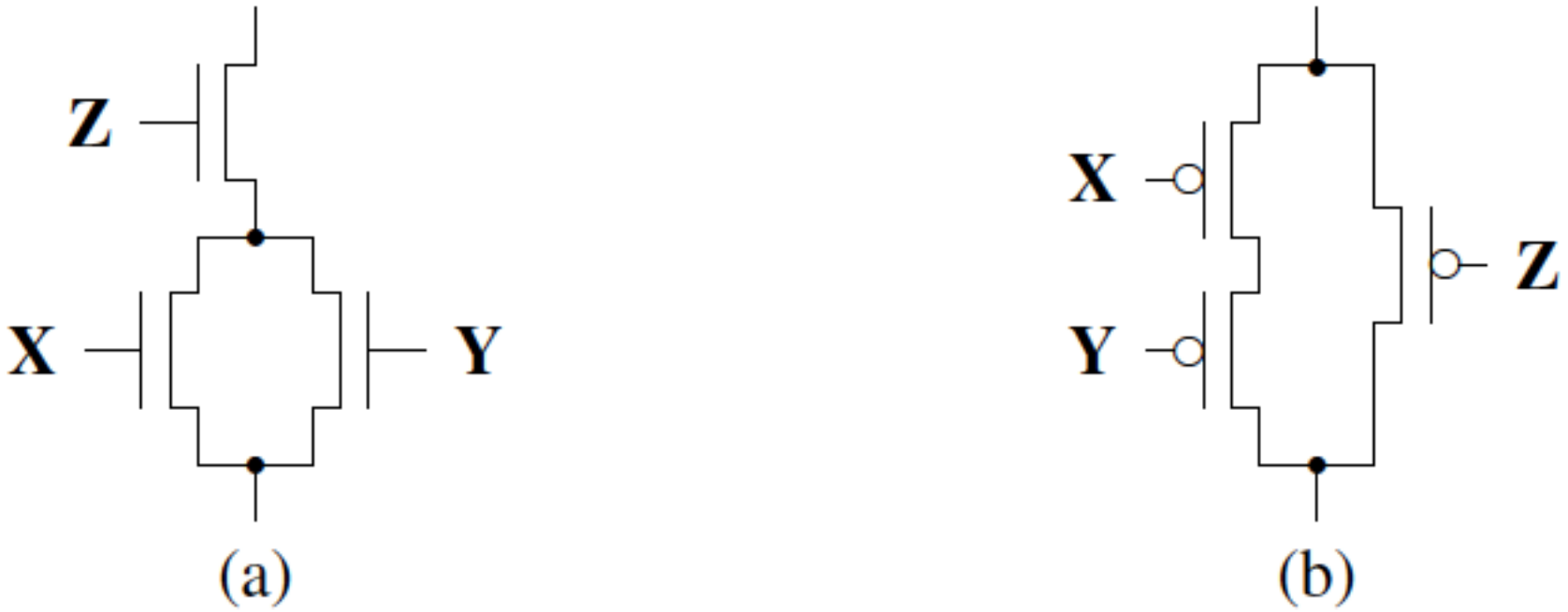
(b)

Complementary structures

- Build the PUP from the PDN or viceversa
- Replace
  - PMOS with NMOS (and viceversa)
  - Parallel branches with series branches (and viceversa)
- Signals going to inputs: unchanged

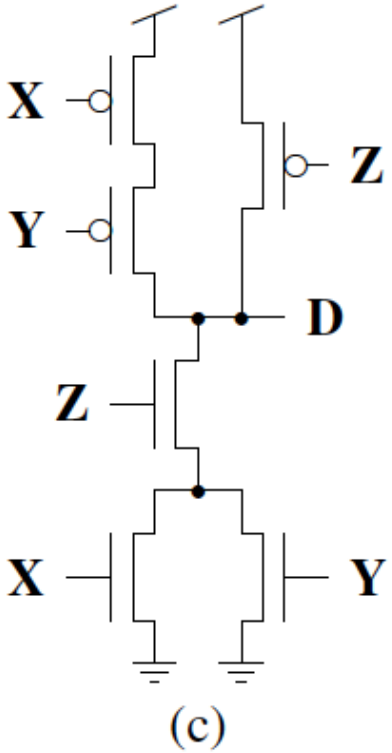
Complementary structures

- Example

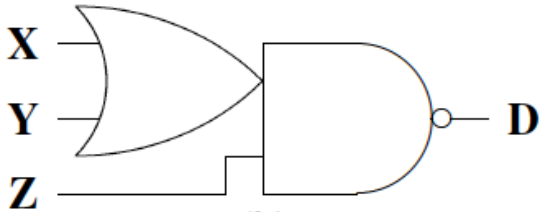


Complementary structures

- Example



(c)

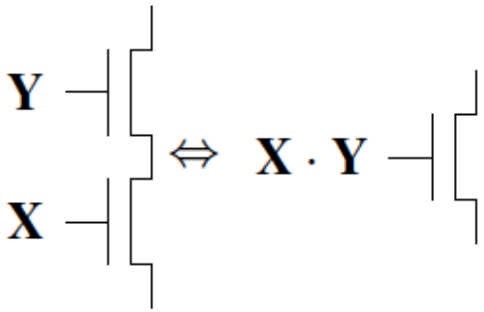


(b)

$$\mathbf{D} = \overline{(\mathbf{X} + \mathbf{Y}) \cdot \mathbf{Z}}$$

Boolean equation method (I)

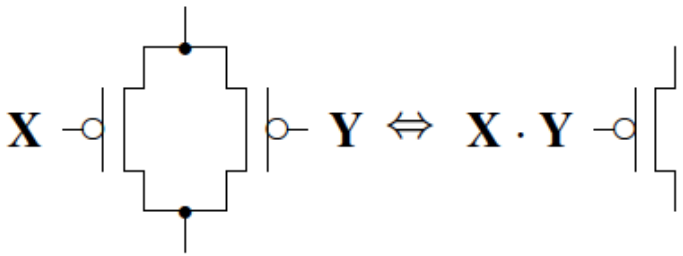
- Any network equivalent to a single FET + Boolean expression



CMOS OUT

X=1 AND y=1 then ON

$\overline{x \cdot y}$

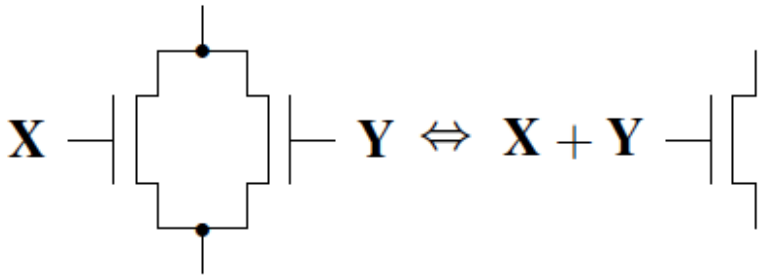


X=0 OR y=0 then ON

$\overline{x} + \overline{y}$

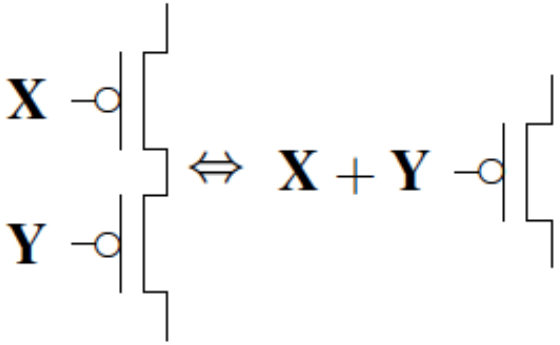
Boolean equation method (II)

- Any network equivalent to a single FET + Boolean expression



CMOS OUT

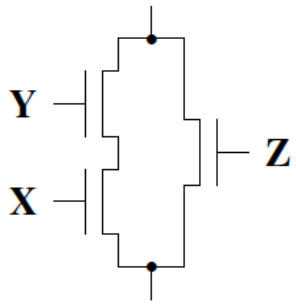
X=1 OR y=1 then ON $\overline{x + y}$



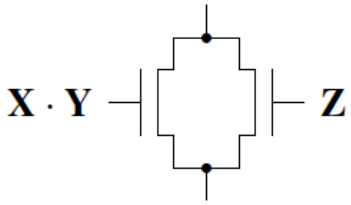
X=0 AND y=0 then ON $\overline{x} \cdot \overline{y}$

Boolean equation method (I)

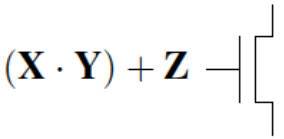
- Reduction



(a)

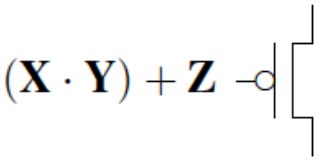


(b)

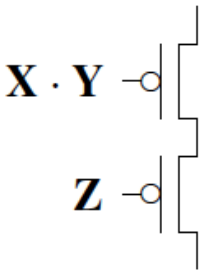


(c)

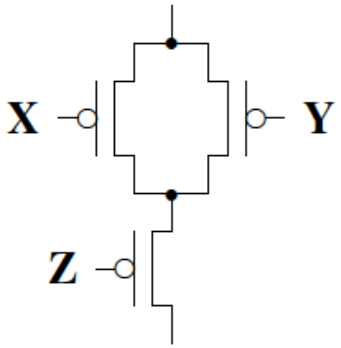
- Expansion



(a)



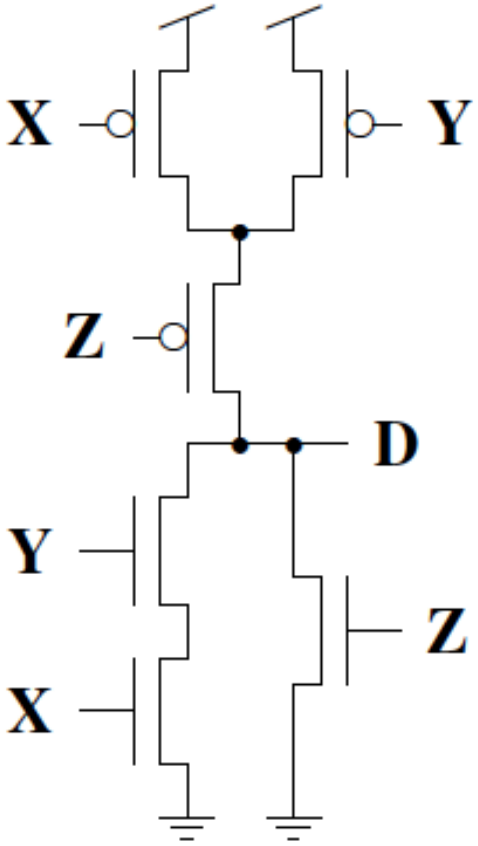
(b)



(c)

Boolean equation method (II)

- Example



(c)

$$D = \overline{(X \cdot Y) + Z}$$

(d)