MOS storage array has been described. This approach appears to be at an early stage in its development and, with appropriate work in this area, the future for this type of memory is bright.

Acknowledgment

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References

[1] J. D. Schmidt, "Integrated MOS transistor random access memory," *Solid State Design*, pp. 21–25, January 1965.
[2] P. Pleshko and L. M. Terman, "An investigation of the potential of MOS transistor memories," *IEEE Trans. Electronic Computers*, vol. EC-15, pp. 423–427, August 1966.
[3] S. Nissim, G. V. Podraza, and D. E. Brewer, "Low power computer memory system," *1967 Fall Joint Computer Conf., AFIPS Proc.* Washington, D. C.: Thompson, 1967, pp. 381–393.
[4] D. Frohman-Bentchkowsky and L. Vadasz, "Computer-aided design and characterization of MOS integrated circuits," *1968 ISSCC Digest of Tech. Papers*, vol. 11.

Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits

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Abstract—**A new equivalent circuit for the insulated-gate field-effect transistor (IGFET) is described. This device model is particularly useful for computer-aided analysis of monolithic integrated IGFET switching circuits. The results of computer simulations using the new equivalent circuit are in close agreement with experimental observations. As an example of a practical application, simulation results are shown for an integrated circuit IGFET memory cell.**

I. Introduction

COMPUTER circuit analysis programs are significant aids to integrated circuit design because they can reduce or eliminate the expense and delay of cut-and-try design approaches [1].

Mathematical approximations, or models, for the electrical characteristics of electronic devices are essential in any circuit analysis procedure. A mathematical model represented by a combination of circuit elements (resistances, capacitances, dependent sources, etc.) is called an equivalent circuit. These representations of mathematical models are not necessary for computer-aided circuit analysis. However, they aid understanding, particularly in the evolution of new circuit and device concepts.

This paper describes a new equivalent circuit for the insulated-gate field-effect transistor (IGFET). The equivalent circuit has been used with good results for computer analysis of the dc and transient characteristics of IGFET switching circuits. Computer-aided analysis techniques have proven particularly useful for IGFET integrated circuits because the behavior of these circuits is often dominated by the nonlinear characteristics of IGFETs and by multiple intradevice capacitances. Manual analysis of IGFET switching circuits usually requires gross approximations that can lead to invalid results.

The new IGFET model is used with a general-purpose circuit analysis program that employs state-variable techniques. The program derives first order differential equations from input data defining circuit topology and device parameters. The dc solution is obtained by setting the derivatives in the differential equations equal to zero, and solving for the steady-state voltages using an iterative function [2]. The transient solution is obtained by numerically integrating the complete set of differential equations. A new technique for numerical integration has been developed to reduce computer running time for circuit analysis [3].

II. Features of the Model

The new IGFET model has several key features that enhance its usefulness in computer-aided analysis of integrated circuits. Separate drain, gate, source, and substrate terminals are available. Full representation of the effect of substrate bias on gate threshold voltage is included. The model is equally applicable to both enhancement-mode and depletion-mode devices, whether

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p-channel or n-channel. Simulation results are valid for any combination of terminal voltages that do not cause electrical breakdown in the actual device.

The number of state variables generated in computer analysis is minimized by making no distinction between "intrinsic" and "parasitic" elements in the equivalent circuit. A minimum number of state variables is desirable to limit the computation time in circuit analysis. This approach has the further advantage of simplying the evaluation of the elements in the equivalent circuit.

Equivalent circuit parameters may be evaluated either with measurements, employing a curve tracer and capacitance bridge, or with direct calculations from device geometry and material parameters. The above combination of features is not available with previously reported IGFET equivalent circuits [4], [5].

III. Device Analysis

The present approach to the modeling problem is influenced by the nature of results desired in simulation and by the typical IGFET geometry in integrated circuit realization. Because large-signal switching and recovery times are the transient characteristics of greatest interest, average values of device capacitances (rather than voltage-dependent representations) can be often used without undue sacrifice of accuracy. However, if necessary, voltage-dependent capacitances may directly replace fixed capacitances in the equivalent circuit and in the computer program.

Fig. 1 shows a typical short-channel IGFET such as is used for switching and gating functions. Half or more of the total gate area overlaps the heavily doped source and drain regions. When the capacitances of metallized wiring and other parasitic elements are included, the distributed gate-channel capacitance of the short-channel device typically comprises less than one third of the total gate node capacitance. In this case, the gate-channel capacitance may be divided equally between the lumped gate-source and gate-drain capacitances. Results shown elsewhere may be used if a more precise treatment is necessary [6].

At first glance, the above approach appears invalid for the long-channel devices sometimes used as high-impedance load elements. The distributed gate-channel capacitance of such devices comprises a large fraction of the total gate node capacitance. However, because the gate of an IGFET used as a load element is tied to a fixed potential, the exact way in which the gate-channel capacitance is modeled has little influence on simulation results. For simplicity, the gate capacitance may be divided as for the short-channel devices.

The foregoing simplifications are further justified when one considers that waveforms at internal nodes of an IGFET integrated circuit are not readily observable because node capacitances are typically of the order of 0.1 pF. At external nodes, packaging and external circuitry largely determine total capacitance loading and hence transient performance. It appears that little additional insight into circuit performance can be obtained by a more detailed representation of gate-channel capacitance in practical IGFET integrated circuit. Moreover, it would be particularly difficult to confirm experimentally the validity of a more elaborate representation.

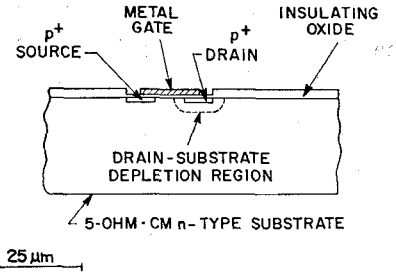

Fig. 1. Cross-sectional view of a typical integrated-circuit IGFET.

Practical IGFETs are observed to have a significant output conductance as a result of channel-length modulation and electrostatic drain-source coupling. An approximate representation of these effects is included in the model.

IV. IGFET Equivalent Circuit

Complete IGFET circuit models are shown in Figs. 2 and 3 for n-channel and p-channel devices, respectively. Resistors R_1 and R_2 represent the series resistance between the ohmic contacts and the active region. R_3 and R_4 are the spreading resistances from source and drain junctions into the substrate region. In many cases, the lumped resistances shown here are only a crude approximation of reality. However, in typical operation, the voltage drops across these elements are so small (in the millivolt range) that they have little effect on circuit performance. C_{GS} and C_{GD} are the two lumped components of gate capacitance, as previously discussed. The value chosen for C_{GS} and C_{GD} is one half of the gate-channel capacitance.

The two diodes represent the junctions between the drain and substrate and between the source and substrate, respectively. The capacitances C_{SD} and C_{SS}, which are drawn in dotted lines, are the depletion capacitances of these junctions. They are shown separately in Figs. 2 and 3 to define the capacitances C_{SD} and C_{SS}, which will be used later. The charge-control diode model shown in Fig. 4 is used to characterize the source-to-substrate and drain-to-substrate junctions [7]. Note that the junction depletion capacitance is a part of the model. The application of the charge-control model permits consideration of minority carrier charge storage, which is present if these junctions become forward biased.

The dependent drain current source I_d represents the current flowing between the drain and source via the

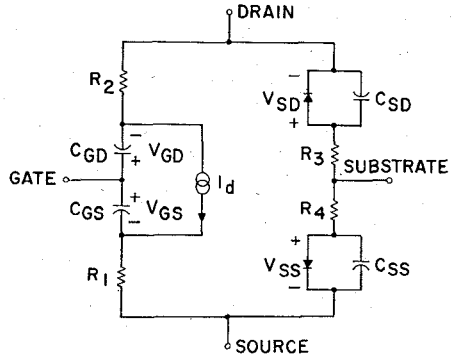

Fig. 2. n-channel IGFET circuit model and polarity conventions.

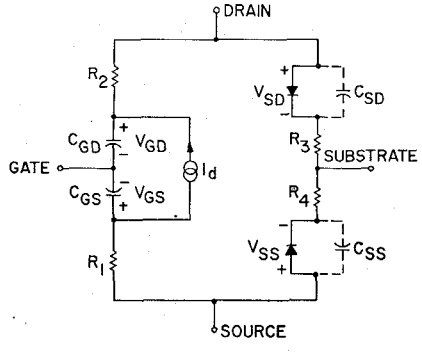

Fig. 3. p-channel IGFET circuit model and polarity conventions.

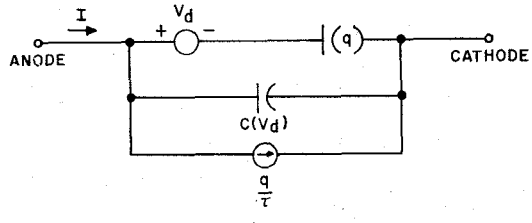

Fig. 4. Charge-control diode model used to represent source-substrate and drain-substrate junctions.

$$V_T = V_{TO} + K_2\left[\left(-V_{SD}+\psi\right)^{1/2} - \psi^{1/2}\right] \Big| V_{SD} > V_{SS}$$
$$= V_{TO} + K_2\left[\left(-V_{SS}+\psi\right)^{1/2} - \psi^{1/2}\right] \Big| V_{SS} > V_{SD}$$
$$I_d = K_1\left(F_1 - F_2\right)\left(1+\mathcal{L}\left|V_{GS}-V_{GD}\right|\right)$$
$$\text{where } F_1 = \begin{bmatrix} 0 & V_{GS} < V_T \\ \left(V_{GS}-V_T\right)^2 & V_{GS} \geq V_T \end{bmatrix}$$
$$F_2 = \begin{bmatrix} 0 & V_{GD} < V_T \\ \left(V_{GD}-V_T\right)^2 & V_{GD} \geq V_T \end{bmatrix}$$
$$K_1 = \frac{\mu C}{2}\frac{W}{L}\,; \quad K_2 = \frac{2\epsilon_S}{\epsilon_i}\left(\frac{N q d^2}{2\epsilon_S}\right)^{1/2}$$

Fig. 5. The dc equations for p-channel and n-channel devices.

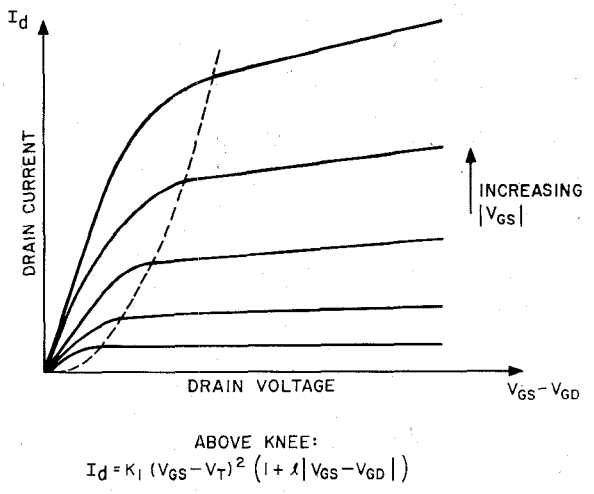

Fig. 6. IGFET drain voltage-current characteristics, showing the effect of channel-length modulation.

channel. The equations relating I_d to the various voltages and material parameters are shown in Fig. 5. The equations were developed from results given elsewhere [8] through a change of variables and through the addition of the term $(1+l|V_{GS}-V_{GD}|)$ to represent channel-length modulation and electrostatic drain-source coupling. Fig. 6 illustrates that these effects result in a finite slope of the characteristic curves, beyond pinchoff, which is proportional to the current at the pinchoff point. A more detailed representation of the drain current source may be used [9]. However, our experience indicates that the equations shown here are adequate for simulation of large signal switching circuits.

The equations in Fig. 5, despite the complexity arising from the conditional equalities, are easily programmed on a digital computer.

V. Experimentation Verification

For confirmation of the validity of the model, the cascaded inverter circuit of Fig. 7 was simulated and the results compared with experimental measurements. The devices used were discrete p-channel enhancement-mode IGFETs having a geometry similar to integrated devices and with a separate substrate contact available at a fourth lead. This permitted a common substrate connection for all devices, as would be found in an integrated circuit. All capacitances, as well as the constants K_1, K_2, V_{TO}, and l were measured. Other device parameters were calculated from device geometry, diffusion specifications, and appropriate physical constants.

The results of the measurements and the predicted response for the output voltage of the cascaded inverter circuit are shown in Fig. 8. The dotted line was obtained experimentally. The solid line was computed using the IGFET model and the circuit analysis program. A single curve shows the input for both the analytical and experimental input signal. It should be noted that no

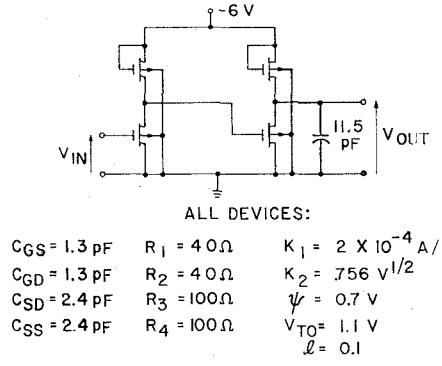

Fig. 7. Cascade of two IGFET inverter stages.

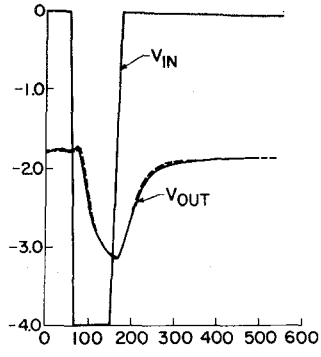

Fig. 8. Measured (dotted trace) and computed (solid trace) switching response of two-stage cascade.

shift of either vertical or horizontal axis was required to obtain the agreement between experimental and analytic curves shown in Fig. 8. The computed output is within 5 percent of the experimental result, which was taken with a chart recorder driven from a sampling oscilloscope. The computer time for this problem was less than one minute using a GE 645.

VI. Practical Application of IGFET Model

Fig. 9 is a photomicrograph of an integrated circuit IGFET memory cell. Fig. 10 is a schematic of the memory cell that shows the IGFET model substituted for three of the devices on the right half of the cell. The 20-pF capacitors and the 6.8-kΩ resistors simulate the loading effect of other components that would be present in a memory system. The predicted performance of the memory cell during the entire read–write cycle is shown in Fig. 11.

The initial conditions are chosen such that the left side of the flip–flop is conducting. The cycle begins when the word line W is brought down to zero volts. Current flows out through the left-hand gating IGFET and begins to charge the 20-pF digit line capacitance. The waveform is shown in the lower left corner of Fig 11. This signal is the input to a detector that generates a logic-level data output pulse.

Following the read operation, a signal is applied to point D to write new information into the cell. The

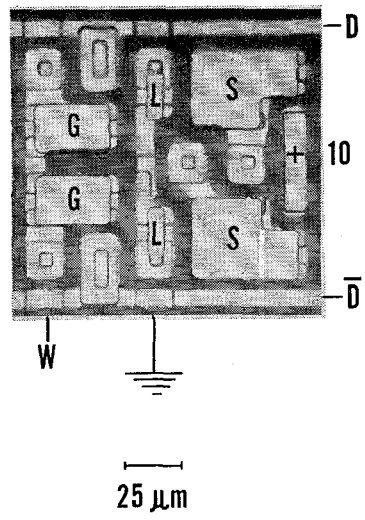

Fig. 9. Photomicrograph of an integrated-circuit IGFET memory cell. Devices are lettered to correspond to letters shown in Fig. 10.

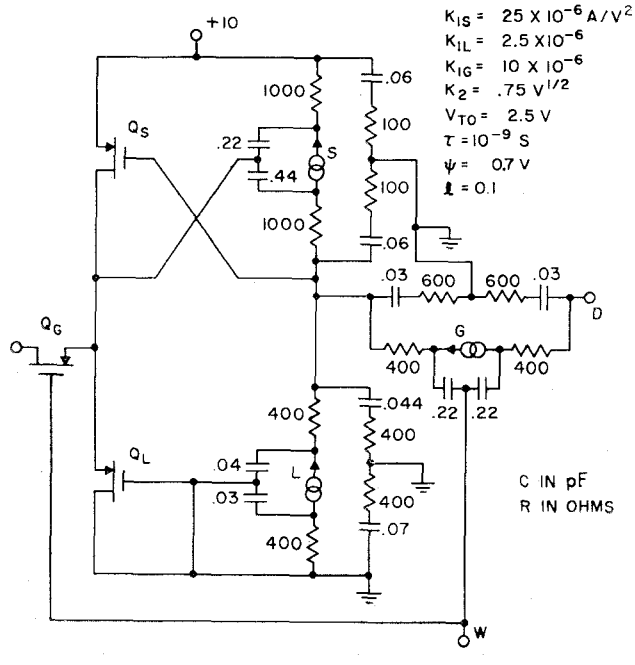

Fig. 10. IGFET memory cell circuit.

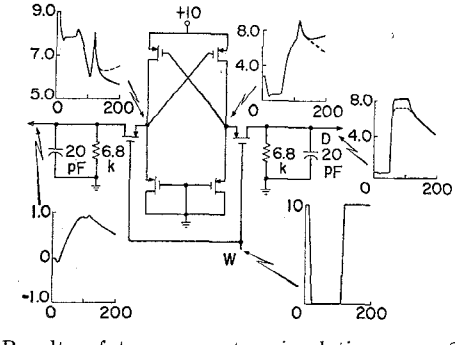

Fig. 11. Results of two computer simulation runs. Solid traces show cell switching; dotted traces show cell returning to original state.

solid traces show the drive signal and response when the desired change of state takes place. The dotted traces show the results of a second simulation in which the drive signal was not adequate to cause the desired change of state.

The cell readout behavior and switching sensitivity, as shown in Fig. 11, have been confirmed by experimental measurements. It should be noted that a direct comparison of experimental and analytical data at internal nodes of this circuit is not practical. The capacitance of a probe would alter significantly the actual circuit response.

Less than three minutes of GE 645 computer time was required to compute each set of curves shown in Fig. 11.

List of Symbols

V_T, V_{TO} = threshold voltage with and without source-substrate bias;
Ψ = channel surface potential $= (2kT/q) \ln(N/n_i)$;
μ = carrier mobility in channel;
C = capacitance per unit area of gate;
W, L = channel width and length;
ϵ_s, ϵ_i = dielectric constants of silicon and of gate insulator;
N = carrier concentration in substrate;
d = gate insulator thickness;
q = electronic charge;
l = channel-length modulation constant;
n_i = intrinsic concentration in substrate.

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References

[1] F. F. Kuo, "Network analysis by digital computer," *Proc. IEEE*, vol. 54, pp. 820–829, June 1966.
[2] J. F. Traub, *Iterative Methods for the Solution of Equations*. Englewood Cliffs, N. J.: Prentice-Hall, 1964.
[3] I. W. Sandberg and H. Shichman, "Numerical integration of systems of stiff nonlinear differential equations," *Bell Sys. Tech. J.*, vol. 47, April 1968.
[4] H. K. J. Ihantola and J. L. Moll, "Design theory of a surface field-effect transistor," *Solid-State Electron.*, pp. 423–430, 1964.
[5] B. D. Roberts and C. O. Harbourt, "Computer models of the field-effect transistor," *Proc. IEEE*, vol. 55, pp. 1921–1929, November 1967.
[6] C. T. Sah and H. C. Pao, "The effects of fixed bulk charge on the characteristics of metal-oxide-semiconductor transistors," *IEEE Trans. Electron Devices*, vol. ED-13, pp. 393–409, April 1966.
[7] D. Koehler, "The charge-control concept," *Bell Sys. Tech. J.*, vol. 46, pp. 523–576, March 1967.
[8] J. T. Wallmark and H. Johnson, Eds., *Field-Effect Transistors*. Edgewood Cliffs, N. J., Prentice-Hall, 1966, pp. 113–155.
[9] D. Froman-Bentchkowsky and L. Vadasz, "Computer-aided design and characterization of MOS integrated circuits," *1968 ISSCC Digest of Tech. Papers*, pp. 68–69.