

Analysis of Oscillatory Metastable Operation of an *RS* Flip-Flop

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Abstract—With continuing advances in VLSI technology, there is a growing interest in large-scale parallel systems with numerous high-frequency asynchronous interactions. However, these interactions may result in frequent failures due to metastable operation of flip-flops used as synchronizers or arbiters. For some flip-flops the metastable operation may be of an oscillatory nature, before finally resolving one of stable states. The purpose of this paper is to present an analysis of this mode of metastable operation based on a modified dynamic *RS* flip-flop model including a low-pass filter and fixed nonzero gate delay block. Analytical formulas for the frequency of the oscillatory metastable operation are derived. Good agreement is observed between the theoretical results, SPICE simulation, and experiments with two CMOS *RS* flip-flops. Failure rate due to oscillatory metastable operation is discussed based on the experimental results.

I. INTRODUCTION

METASTABLE operation is unavoidable in asynchronously controlled flip-flops. Due to the occurrence of this phenomenon, flip-flops used as synchronizers or arbiters in asynchronous systems may suffer from an unusually long time needed to attain a stable state. These added delays lead to digital system malfunctions. A characteristic resolution process from the metastable state to one of the stable states depends upon the flip-flop circuit parameters. For *RS* flip-flops constructed with NOR (or NAND) gates with a small propagation delay-to-rise/fall time ratio, the resolution from metastable state is an exponentially increasing function of time. A number of papers are devoted to the analysis of this kind of metastable operation. When the gate propagation delay time is not negligible in comparison with the rise/fall time, the flip-flop outputs may oscillate a number of times between the ZERO and ONE states before finally coming to rest in one stable state. This oscillatory metastable operation was experimentally observed in TTL flip-flops [1]–[3], CMOS flip-flops with double-buffered output stages [6], [7], and can be expected in flip-flops made in any technology. For scaled-down NMOS, CMOS, or Bi-CMOS technology, a propagation delay along interconnection paths between the cross-coupled pairs may also result in oscillatory metastable operation.

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Apart from experimental observation, no theoretical analysis of the oscillatory metastable operation is available in the literature. In this paper an *RS* flip-flop is modeled by adding a fixed time-delay block to a standard equivalent circuit (of NOR or NAND gates). The oscillatory solution in metastable operation is investigated based on this model, which is described by a system of two differential-difference equations with retarded argument. The frequency of oscillation is derived in implicit form as a function of the flip-flop circuit parameters, such as voltage gain in a transition region of transfer characteristic and the rise/fall-to-delay time ratio of NOR gates. Good agreement between the theoretical analyses with SPICE simulation and experiments validates the flip-flop model presented in the paper. Failure rate due to oscillatory metastable operation is discussed based on experiments.

II. A MODIFIED *RS* FLIP-FLOP MODEL

Fig. 1 shows a dynamic model for the standard *RS* flip-flop with NOR gates. The gates are assumed to be identical. Each gate is modeled by the continuous zero memory transfer function $F(X, Y)$, followed by fixed nonzero time-delay block τ and *RC* low-pass filter, both representing the inertia of the NOR gate. This model is more generalized compared to models presented in [4] and [5]. Metastable operation of this flip-flop occurs when voltages at two inputs *S* and *R* are going low simultaneously and next stay at low voltage level for a long time (this kind of *RS* flip-flop excitation is called idle inputs [4]). For the condition $V_S(t) = V_L$ and $V_R(t) = V_L$, $t \geq 0$, the flip-flop behaves like an autonomous system whose dynamic is described by the following nonlinear differential-difference equations:

$$RC \frac{dV_Q}{dt} + V_Q = F[V_L, V_{\bar{Q}}(t - \tau)] \quad (1a)$$

$$RC \frac{dV_{\bar{Q}}}{dt} + V_{\bar{Q}} = F[V_L, V_Q(t - \tau)]. \quad (1b)$$

The system in (1) possesses three equilibrium points—two of them are stable and one is unstable. A graphic interpretation of these points on a phase plane $(V_Q, V_{\bar{Q}})$ is shown in Fig. 2. We are interested in a solution of the system (1) around the unstable point P_3 , which corre-

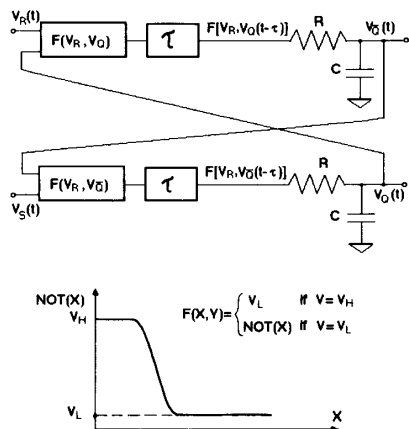


Fig. 1. Modified dynamic model for standard RS flip-flop.

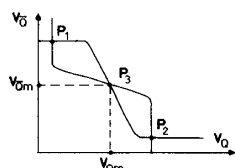


Fig. 2. Equilibrium points of RS flip-flop.

sponds to the metastable state of the flip-flop. The solution may be explored by substituting $V_{\bar{Q}} = V_{\bar{Q}_m} + u$ and $V_Q = V_{Q_m} + v$, where u and v are small variations. Using Taylor expansion of the right-hand sides of (1) and leaving the linear terms only, one can transform the nonlinear system (1) to the system of linear equations for variables v and u :

$$RC \frac{dv}{dt} + v = -Gu(t - \tau) \quad (2a)$$

$$RC \frac{du}{dt} + u = -Gv(t - \tau) \quad (2b)$$

where $-G$ is the small-signal voltage gain of the NOR gate at the operating point V_{Q_m} or $V_{\bar{Q}_m}$. ($V_{Q_m} = V_{\bar{Q}_m}$, since the flip-flop circuit is assumed to be symmetrical.)

When combined, (2a) and (2b) lead to a single second-order differential equation with retarded argument 2τ :

$$a^2 \frac{d^2 u}{dt^2} + 2ab \frac{du}{dt} + b^2 u - u(t - 2\tau) = 0 \quad (3)$$

where $a = RC/G$ and $b = 1/G$; $a, b > 0$. If a solution of (3) is assumed in the form of $u(t) = A \exp(\Omega t)$, where A is a constant dependent on the initial condition and Ω is complex, the resulting characteristic equation is

$$a^2 \Omega^2 + 2ab\Omega + b^2 - \exp(-2\Omega\tau) = 0. \quad (4)$$

The form of roots of the characteristic equation (4) determines the form of solutions of (3). Since (4) involves the transcendental function $\exp(-2\Omega\tau)$, an infinite number of

roots are possible. The roots and their location on a complex plane depend on a , b , and τ (R , C , G , and τ). Hence, the relationship between roots of the characteristic equation and parameters of the flip-flop circuit gives conditions for oscillatory or nonoscillatory metastable operation.

III. OSCILLATORY SOLUTION

In this section possible solutions of (3) are investigated. This is done through the analysis of existence of roots [8] of the characteristic equation (4). The simplest case is where these roots are real only. Graphically, the solution for real roots is given in Fig. 3. For $b > 1$ ($G < 1$), two negative roots Ω_1 and Ω_2 exist leading to an asymptotically stable solution of (3). In practice this case is not of interest, since the voltage gain of a physical NOR gate must be greater than 1. When $b = 1$ ($G = 1$), (4) possesses trivial root $\Omega = 0$ which corresponds to constant solution of (3), i.e., $u(t) = \text{constant}$. For $b < 1$ ($G > 1$) the root Ω_1 becomes positive. This leads to an unstable solution of (3) which has the form of an exponentially increasing function of time and corresponds to the nonoscillatory resolving phase of the flip-flop metastable operation. This solution may exist for $\tau \geq 0$.

If oscillatory solution of (3) exists, Ω becomes a complex number. The simplest possibility is that the solution has the form of steady-state oscillation which corresponds to pure imaginary root $\Omega = j\omega$. In this case (4) gives two equations for real and imaginary parts:

$$-a^2\omega^2 + b^2 - \cos(2\omega\tau) = 0 \quad (5a)$$

$$2ab\omega + \sin(2\omega\tau) = 0. \quad (5b)$$

Oscillation is possible if both (5a) and (5b) have the same solution for ω . This solution exists only while $|-a^2\omega^2 + b^2| < 1$ and $|2ab\omega| < 1$.

In solving (5a) and (5b) for variables a and b , one gets two formulas expressed in terms of ω and τ :

$$a = -\sqrt{\frac{2}{1 + \cos(2\omega\tau)}} \cdot \frac{\sin(2\omega\tau)}{2\omega} > 0, \quad \text{for } k\pi < 2\omega\tau < (k+1)\pi, \quad k = 1, 3, 5 \dots \quad (6a)$$

$$b = \sqrt{\frac{1 + \cos(2\omega\tau)}{2}} > 1, \quad \text{for } 2\omega\tau > 0. \quad (6b)$$

The only case of practical interest is that where just the lowest possible frequency of oscillation exists. The lowest possible range of $2\omega\tau$ in which (6a) and (6b) are satisfied is for $k = 1$, i.e. $\pi < 2\omega\tau < 2\pi$. Given the flip-flop parameters—voltage gain G , low-pass filter time constant RC , and time delay τ —the frequency of oscillation ω in metastable operation may be derived solving (6a) and (6b) simultaneously. When (6a) and (6b) are satisfied for given a , b , and τ , the frequency of oscillation is done in the

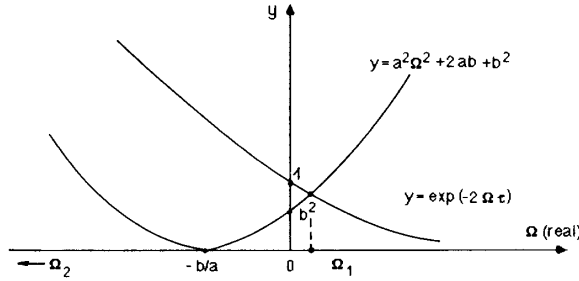


Fig. 3. Graphic solution for the real roots of (4).

following form:

$$\omega = 2\pi f = \frac{\sqrt{G^2 - 1}}{RC}. \quad (7)$$

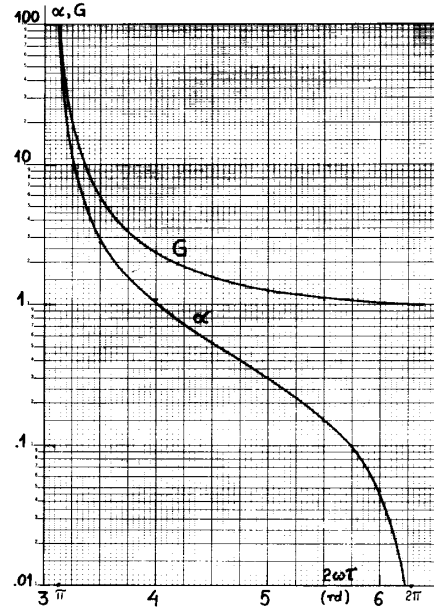
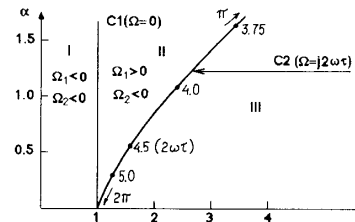
Combining the RC constant and the time delay τ into a new variable defined as $\alpha = RC/\tau$ with $\tau > 0$, one can analyze imaginary roots of the characteristic equation (4) on the plane α - G . Transforming (6a) and (6b) the formulas for α and G can be derived in terms of $\omega\tau$:

$$\alpha = -\frac{2}{1 + \cos(2\omega\tau)} \cdot \frac{\sin(2\omega\tau)}{2\omega\tau} > 0, \quad \text{for } \pi < 2\omega\tau < 2\pi \quad (8a)$$

$$G = \sqrt{\frac{2}{1 + \cos(2\omega\tau)}} > 1, \quad \text{for } \pi < 2\omega\tau < 2\pi. \quad (8b)$$

The graphs of (8a) and (8b) are shown in Fig. 4. The formulas (8a) and (8b) represent parametric equations (with $2\omega\tau$ as the parameter) of the contour C_2 (root locus) on the plane α - G (see Fig. 5). At this contour (4) possesses pure imaginary roots and (3) has a stable oscillatory solution. Values of $2\omega\tau$ at certain points on this contour are shown. When the NOR-gate delay time τ is much greater than its rise or fall time (the rise or fall time is proportional to the RC constant of the low-pass filter, Fig. 1), the coefficient α becomes very small ($\alpha \rightarrow 0$) and the parameter $2\omega\tau$ increases to 2π . This means that the frequency of oscillation increases to maximum $f = 1/2\tau$. The voltage gain G must be minimum 1 to maintain the stable oscillation for $\alpha \rightarrow 0$. When the rise or fall time is much greater than the gate delay time τ ($\alpha \rightarrow \infty$) the stable oscillation appears for higher values of the voltage gain G and the frequency of oscillation decreases to minimum $f = 1/4\tau$. For any other combination of α and G on the root locus C_2 the frequency of oscillation is in the range $1/4\tau < f < 1/2\tau$.

The contour C_1 on Fig. 4 represents the locus of trivial root $\Omega = 0$. The two contours C_1 and C_2 divide the plane α - G ($\alpha > 0, G \geq 0$) into three regions. In region I two negative real roots of (4) exist: one has finite value while the other is located in infinity. In region II one of these roots becomes positive. In region III the roots of (4) acquire a positive real part in addition to its imaginary

Fig. 4. Coefficients α (8a) and G (8b) as a function of $2\omega\tau$.Fig. 5. Relationship between the roots of (4) and the coefficients α and G .

part and the solution of (3) is oscillation with amplitude growing to infinity.

IV. VERIFICATION WITH SPICE SIMULATION AND EXPERIMENT

The analysis provided in Section III is limited to the linear model of the RS flip-flop initially hanging at the metastable equilibrium point. In practice a nonlinear limiting action always takes place, reducing the effective gain of the NOR gate as the amplitude of oscillation increases. Ultimately, a steady state is achieved where the effective amplification is just sufficient to maintain oscillation. To determine how good the prediction of the frequency of oscillatory metastable operation obtained by means of the results of Section 3 really is, two CMOS RS flip-flop circuits composed of two buffered NOR gates were tested. The first flip-flop was made with eight NMOS and eight PMOS transistors of four chips CA3600E (CMOS transistor arrays). The circuit schematic of the NOR gate followed by two buffers and the RS flip-flop is shown in Fig. 6. The second RS flip-flop was constructed with two NOR

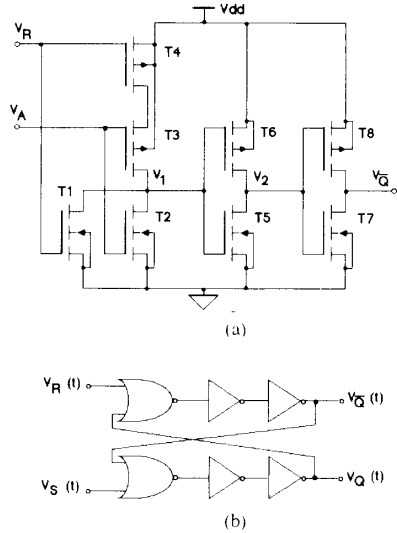


Fig. 6. (a) CMOS NOR gate with two buffer stages, and (b) RS flip-flop.

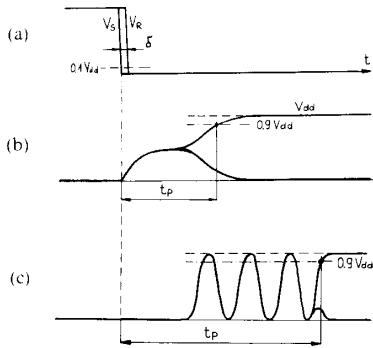


Fig. 7. (a) Definition of the input timing δ ; (b) definition of the propagation delay time t_p for nonoscillatory; and (c) oscillatory metastable operation.

gates of one chip MC14001B (the circuit schematic is the same as given in Fig. 6).

The flip-flop under test was driven at the inputs by two pulses $V_R(t)$ and $V_S(t)$ changing from high to low voltage level with time delay between falling edges δ , called input timing (see Fig. 7(a)). Input signals were provided from two monostables triggered by an external clock. The pulse duration of the first monostable (signal V_R) was kept constant while the pulse duration of the second one (signal V_S) was controlled externally to achieve different input timing δ (δ is assumed to be positive when the transition from high to low voltage level of the pulse V_R lags behind the transition of the pulse V_S). The fall time of the pulses V_R and V_S was less than 5 ns.

Fig. 8(a) shows the real-time oscilloscope display of the output waveforms of the first flip-flop for two cases of input timing, $\delta = 50$ ns and $\delta = 0$ ns. For input timing $\delta = 50$ ns the waveform V_Q is nonoscillatory, while the waveform $V_{\bar{Q}}$ is a short single shot. The energy from this shot is too small to change the flip-flop state, therefore the

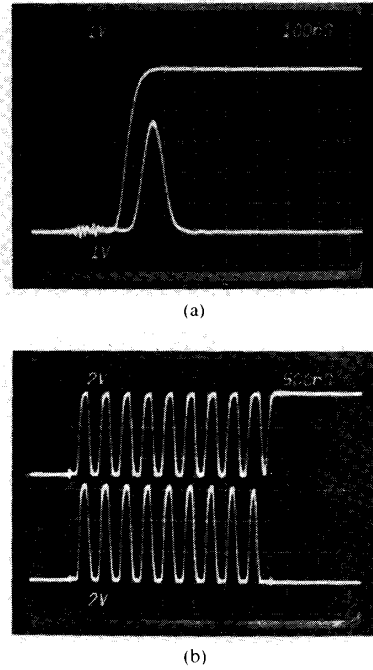


Fig. 8. Real-time oscilloscope output waveforms of the first CMOS RS flip-flop (with chip CA3600E) for input timing (a) $\delta = 50$ ns, 100 ns/div, 1 V/div, and (b) for $\delta = 0$ ns (oscillatory metastable operation), 500 ns/div, 2 V/div.

flip-flop sets within nominal propagation delay time t_{pn} . For input timing $\delta = 0$ with noise-free conditions and perfect symmetry of the circuit, a nonvanishing oscillation should be observed. However, these conditions cannot be maintained in practice. Therefore, Fig. 8(b) shows only several oscillations of V_Q and $V_{\bar{Q}}$ followed by the flip-flop resolution in the metastable state. The frequency of oscillation as measured from the Fig. 8(b) is 2.8 MHz.

SPICE simulation of a step response of one NOR gate with two buffers is presented in Fig. 9. For this simulation a MOSFET model Level 1 (channel length of MOS devices of chip CA3600E is much greater than $2 \mu\text{m}$) was used with dc parameters extracted from measurements (Appendix) and with component capacitances taken from an RCA catalog. These parameters are summarized in Table I. Fig. 9 shows a construction for determining an average value of RC constant and an average value of time delay τ . These values are $RC = 42$ ns and $\tau = 131$ ns, which gives the value of the parameter $\alpha = (42/131) = 0.321$. From (8a) or directly from the plot in Fig. 4, oscillation in the metastable state exists for $2\omega\tau = 4.95$ rad. The average large-signal gain G for this point is about 1.27. Having the value of $2\omega\tau$, one can calculate a real frequency from the formula $f = 2\omega\tau / (4\pi\tau) = 4.95 / (4 \times \pi \times 131 \times 10^{-9}) = 3$ MHz. Figs. 10 and 11 show SPICE simulations of the flip-flop metastable operation for input timing $\delta = 50$ ns and $\delta = 10$ ns. Only two periods of outputs V_Q and $V_{\bar{Q}}$ for $\delta = 10$ ns are shown since the flip-flop resolves next to a stable state. The frequency of oscillation is 2.5 MHz, which is in good

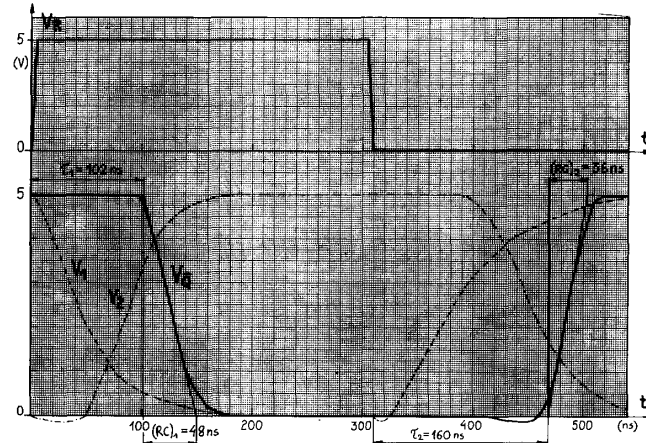


Fig. 9. SPICE simulation of the step response of CMOS NOR gate with two buffers (constructed with chip CA3600E).

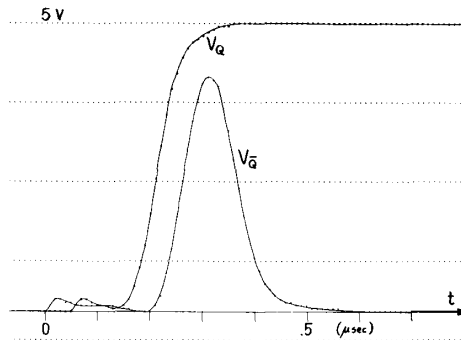


Fig. 10. SPICE simulation of the first CMOS RS flip-flop (with chip CA3600E) response for input timing $\delta = 50$ ns.

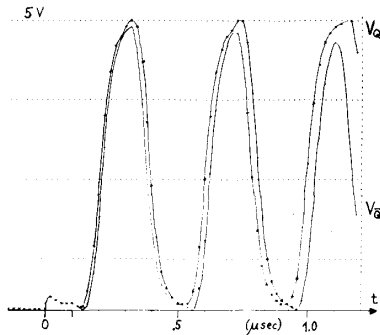


Fig. 11. SPICE simulation of the first CMOS RS flip-flop (with chip CA3600E) response for input timing $\delta = 10$ ns (oscillatory metastable operation).

agreement with the 3-MHz value predicted analytically and with the 2.8-MHz value extracted from Fig. 8(b).

In Fig. 12 a real-time oscilloscope display of the second CMOS RS flip-flop under test (MC14001B) for input timing $\delta = 30$ ns and for $\delta = 0$ ns is presented. The frequency of oscillation in the metastable state is 5.9 MHz. From the oscillogram in Fig. 12(a), the time delay τ and

TABLE I
PARAMETERS OF SPICE MODEL LEVEL 1 FOR NMOS AND PMOS
OF THE CHIP CA3600E

Parameter	NMOS	PMOS
V_{T0} (V)	+1.5	-1.5
β (mA/V ²)	0.40	0.48
GAMMA, γ (\sqrt{V})	2.20	0.70
LAMBDA, λ (V ⁻¹)	0.010	0.017
PHI, ϕ (V)	0.6	0.6
C_{gs} (pF)	6.15	6.60
C_{gd} (pF)	1.35	1.75
C_{db} (pF)	2.65	3.25

the RC constant were extracted using the same construction as in Fig. 9, giving $\tau = 65$ ns and $RC = 40$ ns. The parameter $\alpha = (40/65) = 0.615$, hence from the plot in Fig. 4 one gets $2\omega\tau = 4.30$ rad, and the real frequency of oscillation is $f = 2\omega\tau/(4\pi\tau) = 4.30/(4 \times \pi \times 65E-9) = 5.26$ MHz. The frequency predicted is in good agreement with measurements. SPICE simulation had not been carried out since no transistor parameters were available for this chip.

In designing VLSI digital systems with synchronizers and arbiters, the failure rate due to flip-flop metastable operation is an important issue. To investigate this problem for RS flip-flops under test a suitable propagation time delay t_p was introduced. The conventional definition of the propagation delay time measured at $0.5V_{dd}$ reference point is ambiguous in light of metastable operation since the metastable voltage V_m is very close to $0.5V_{dd}$. Therefore, t_p is defined as the time between when the first input waveform goes low (V_S or V_R) at the reference value $0.1V_{dd}$ and the time when the output voltage waveform (V_Q or $V_{\bar{Q}}$) enters and remains a logic region high at the reference value $0.9V_{dd}$. This definition for nonoscillatory and oscillatory metastable operation is shown in Fig. 7(b)

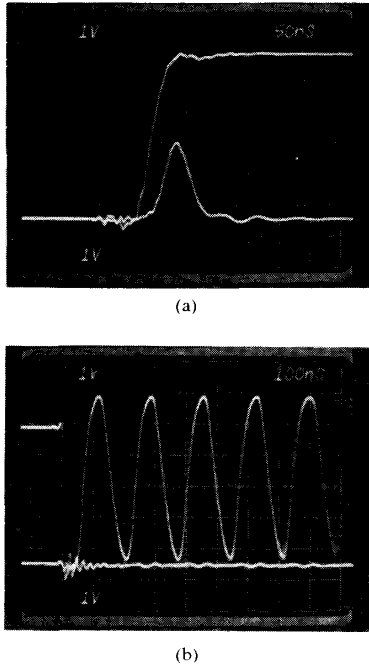


Fig. 12. Real-time oscilloscope output waveforms of the second CMOS RS flip-flop (with chip MC14001B) for input timing (a) $\delta = 30$ ns, 50 ns/div, 1 V/div, and (b) for $\delta = 0$ ns (oscillatory metastable operation), 100 ns/div, 1 V/div.

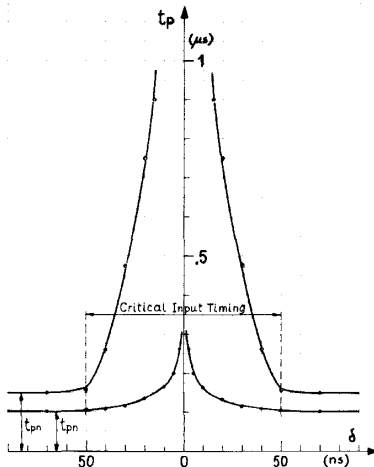


Fig. 13. Propagation delay time t_p versus input timing δ for the CMOS RS flip-flop (with chip CA3600E) without buffers (—●—●—) and with buffers (—○—○—○—).

and (c), and reflects a so-called “length of metastable operation.”

The flip-flop propagation delay time t_p under metastable operation depends on input timing δ . Analytical derivation of this dependence is difficult since it requires a solution of nonautonomous nonlinear equation (1) for given input timing δ . This derivation needs a separate rigorous analysis. Instead, the propagation time t_p versus

input timing δ was obtained experimentally for the first CMOS RS flip-flop under test (CA3600E) with buffer and without buffer (Fig. 13). For input timing -50 ns $< \delta < +50$ ns both flip-flops undergo metastable operation and their propagation delay time t_p exceeds normal (or nominal) propagation delay time t_{pn} . This range of input timing δ is called critical input timing (CIT). When the δ is greater than the CIT the RS flip-flop always sets or always resets within the normal propagation delay time t_{pn} . One must observe that for given input timing δ within CIT the propagation delay time t_p of the flip-flop with buffers is much greater than the t_p of the flip-flop without buffers. This leads to the conclusion that, other things being equal, the nonzero inertial time delay τ of the NOR gate increases the failure rate of RS flip-flops in asynchronous applications. Analysis of the key circuit parameters affecting the failure rate in this new RS flip-flop model needs separate work.

V. CONCLUSION

The modified RS flip-flop model for which a dynamic behavior of its NOR gate components is represented by low-pass filter with the inclusion of inertial delay turned out to be a good system for the analysis of oscillatory metastable operation. The system is described by two differential-difference equations. The oscillatory solution was investigated based on the distribution of roots in the characteristic equation. The condition for oscillatory metastable operation depends on the characteristic rise/fall-to-delay time ratio and voltage gain of the component NOR gates. Correctness of the frequency of oscillation prediction in metastable state was confirmed by experimental observation of two test CMOS RS flip-flops and by SPICE simulation. The probability of failure due to oscillatory metastable operation was also discussed. It is hoped that the analysis presented here will be useful in better understanding the anomalous behavior of flip-flops and will be helpful in developing effective optimization techniques for a VLSI flip-flop design subject to minimum failure rate due to metastable operation in asynchronous digital systems.

APPENDIX EXTRACTION OF MOSFET PARAMETERS FOR SPICE MODEL LEVEL 1

The four parameters of the Schichman–Hodges model [9] (model Level 1 for SPICE)—extrinsic transconductance parameter β , zero-bias threshold voltage V_{T0} , body-effect parameter γ , and channel-length modulation parameter λ —were extracted from the following dc characteristics:

- 1) transfer characteristic $I_D = f(V_{GS})$ measured in the saturation region for $V_{DS} = \text{constant}$ and for different V_{BS} ; and
- 2) output characteristic $I_D = f(V_{DS})$ measured for $V_{BS} = 0$ V and for different V_{GS} .

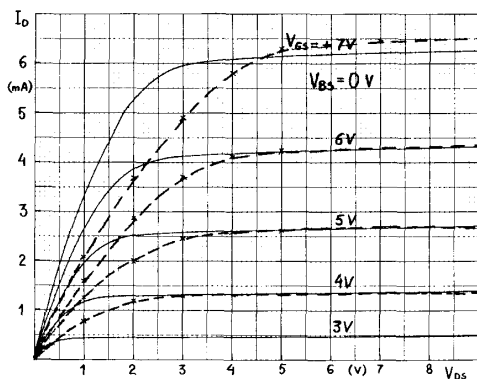


Fig. 14. The NMOS (CA3600E) output characteristics: measurements (—) and SPICE model Level 1 (---).

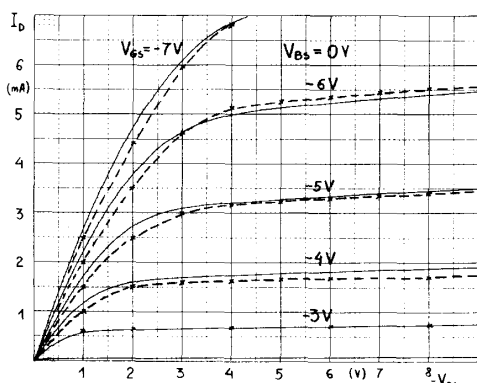


Fig. 15. The PMOS (CA3600E) output characteristics: measurements (—) and SPICE model Level 1 (---).

Based on the transfer characteristics a companion function $\sqrt{I_D} = f(V_{GS})$ was calculated for different values of the voltage V_{BS} . The parameters β and V_{T0} were extracted from the slope and interception point with V_{GS} voltage axis of this function for $V_{BS} = 0$ V. Extrapolated values of threshold voltage were obtained from the interception points for different V_{BS} . Assuming that Fermi potential (PHI) was 0.6 V, the threshold voltage was calculated next as a function of the variable $\sqrt{V_{BS} + 0.6}$ V. From the slope of the plot $V_T = f(\sqrt{V_{BS} + 0.6})$ the approximate value of γ was extracted. The parameter λ was calculated from the slope of the output characteristic for one value of V_{GS} . Sets of NMOS and PMOS parameters of the model Level 1 extracted from measurements of the chip CA3600E are given in Table I. In Figs 14 and 15 a comparison of measurements and SPICE calculations of the output characteristics are shown. It is evident from the figures that the

model is correct as long as the saturation region is considered. Since most of the transistors of the CMOS RS flip-flop operate in saturation when the flip-flop is in the metastable state, the transistor model parameters extracted as above are quite acceptable for SPICE simulation.

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