22.7 Powder LSI: An Ultra Small RF Identification Chip for Individual Recognition Applications

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Product manufacture and distribution requires accurate inventory control of high quality. The μ-chip, a small inexpensive chip with a radio frequency identification (RFID) [1] can be attached to paper media and other small goods, for counterfeit prevention and product tracking in markets. Reduced cost and increased mechanical stress endurance, achieved by continually reducing chip size, are indispensable in these markets. Recent CMOS process technology makes possible the reduction of a μ-chip to 0.3mm x 0.3mm. However, the cost of an RFID device, consisting of the chip and its attached antenna, still depends on assembly complexity.

For RFID, batteryless circuit techniques are widely used for lowering cost and reducing pollution. A simplified block diagram of the developed chip is shown in Fig. 22.7.1. In order to design small, low-power circuitry and reduce semiconductor cost, an available 0.18μm CMOS fine standard process is adopted. Therefore the front end of this chip is designed with a fully CMOS rectifier circuit that enables 2.45GHz operation instead of a special process device such as a Schottky diode. The power rectifier circuit supplies Vdd of 0.5V and the minimum required current of 3μA. One of two input ports is directly connected to a PMOS capacitor. A full swing input signal is imposed at this input capacitor where electrons are transferred to the MOS gate capacitor array of the next stage. The 80pF MOS gate capacitor array stores electrons to power internal circuit operation. A voltage limiter operates when the supply voltage exceeds 2.1V. The clock generator has a function to modulate and demodulate a 2.45GHz carrier to a 100 kHz clock. At the first edge of the clock, power at the reset circuit outputs activates a 10b counter. The output of the 128b ROM is connected to a load switch that enables to the impedance between the input ports to change.

Two new technical problems occur when an ultra small chip is fabricated. One is that handling difficulty increases in inverse proportion to chip size, and the other is precise positioning of the chip with small surface bumps onto an external antenna's metal terminals. Figure 22.7.2 shows a comparison of a conventional input device's structure to that of the developed chip. The conventional type is widely used for all-wave rectification circuits. The inputs are connected to active MOS transistor gates, which compels placing both input electrodes on the same chip surface. This chip's connection structure is simplified so that a two-surface connection structure places only one connection electrode port on each chip surface. This structure is derived from the principle that an RFID chip needs two ports for attaching an external antenna's terminals.

This ultra small RFID chip is mounted on a thin antenna metallic film as illustrated in Fig. 22.7.3. The chip is mounted on the center of the antenna. Because of the two-surface connection the surface connection electrodes are connected to the antenna material by using a sandwich-connection. Precise positioning is not necessary for mounting the ultra small chips to the antenna terminals, because there is only one connection on each surface. Moreover, the chip does not require horizontal direction regularity for mounting and it can be mounted upside-down. This flexibility makes possible the mounting of many chips onto many antenna patterns designed on a substrate film, i.e., a 50 x 50 pattern-matrix. Another advantage of having a two-surface connection is that each connection area is designed to be as large as the chip surface to reduce connection resistance and enhance connection reliability. Thinning the chip to 60μm and a thin anisotropic conductive film (ACF) connection technique are used to fabricate a thin 100μm RFID device for versatile individual recognition applications with thin media such as paper.

Input impedance of the chip is a relatively low 60Ω, which is required to achieve impedance-matching between the chip and the antenna by tuning an impedance-matching slit's length. Figure 22.7.4 shows the communication distance's dependence on the slit length. At the slit length of 8mm, maximum communication distance of 300mm is achieved given a reader output power of 300mW and a reader antenna gain of 13dBi. To keep the performance within the communication range, the slit's length is changable and tuned by a trimming mechanic e.g. a laser beam cutting machine according to the input impedance of the chip.

Another achievement to implementing the small two-surface connection chip is to use conventional glass molded diode assembly technology, as shown in Fig. 22.7.5. Here, the lead wire metal is diverted to an RFID chip antenna.

Figure 22.7.6 shows a comparison of RFID inlet costs. Here, inlet means the intermediate fabrication unit of the device, which consists of the chip and its antenna's substrate. For a conventional connection [2] (small chips with a single-surface connection on one side), assembly cost is the largest portion of the whole cost chip and antenna materials are inexpensive. For small chips with connection on a single-surface, the area of connection and the gap between connections on the chip surface are smaller and narrower than those of large chips; this requires expensive high-precision and/or low-throughput assembly machines. However, in this two-surface connection design, the assembly mechanics are able to handle many small chips at without regard for the surface direction of the chips. These advantages result in increased throughput and drastically lower assembly cost.

Figure 22.7.7 is a microphotograph of the chip. The circuit active area of the top surface is almost covered by an Au bump.

Acknowledgements

The authors would like to express special appreciation to S. Asai and A. Isobe of Hitachi for encouraging this research and to thank Y. Tsunemi, K. Takaragi, A. Nakano, H. Hayakawa, F. Murai, M. Shinagawa, T. Hamagishi,, N. Yamamoto, T. Ookuma, E. Tanba,, M. Ashizawa, A. Horiguchi, and T. Tase for their significant contributions to this research and development work.

References

[1] K. Takaragi, et al., "An Ultra Small Individual Recognition Security Chip," *IEEE Micro,* vol. 21, no. 6, pp. 43-49, Nov/Dec. 2001.

[2] F. -J. Baggerman, et al., "Low-Cost Flip-Chip on Board," *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B.* vol. 19, no. 4, pp. 736-746, Nov. 1996.

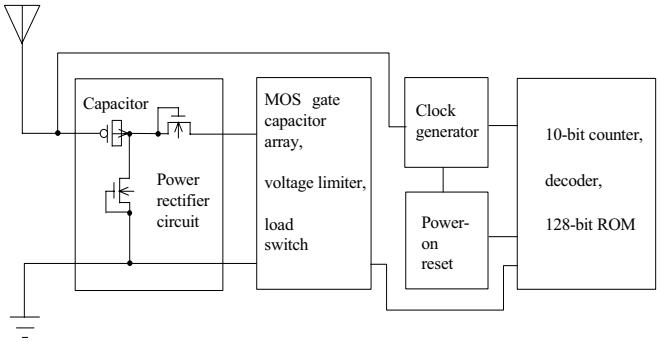

Figure 22.7.1: Block diagram and power rectifier circuit of the chip.

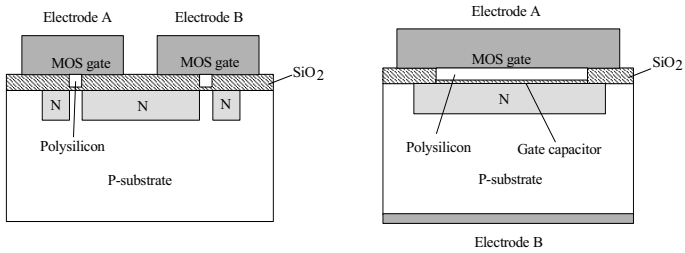

Figure 22.7.2: Simplified input device structure comparison.

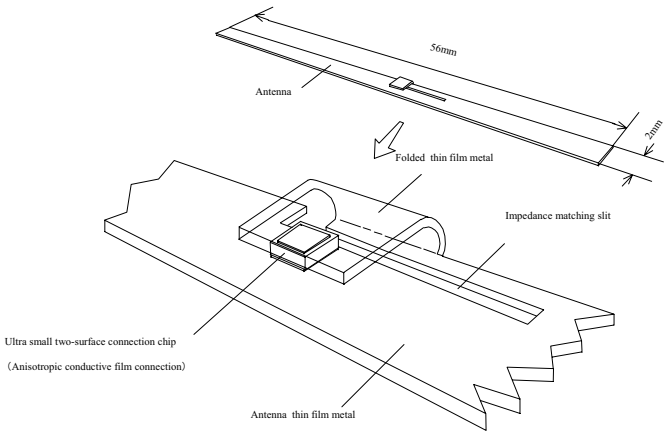

Figure 22.7.3: Connection structure of two-surface connection chip.

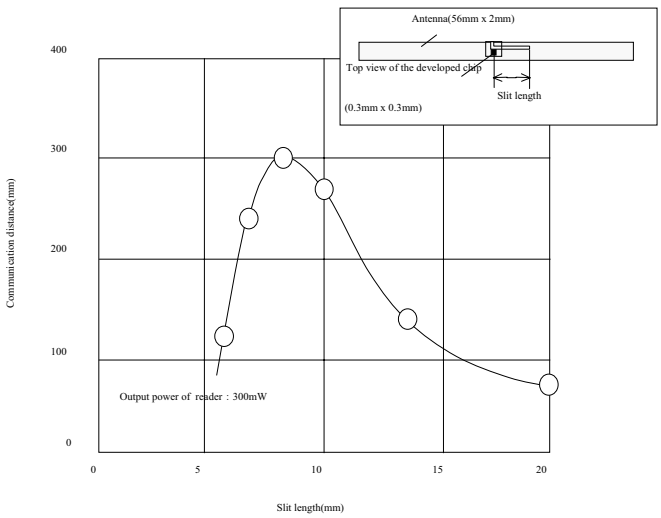

Figure 22.7.4: Communication distance depending on slit length.

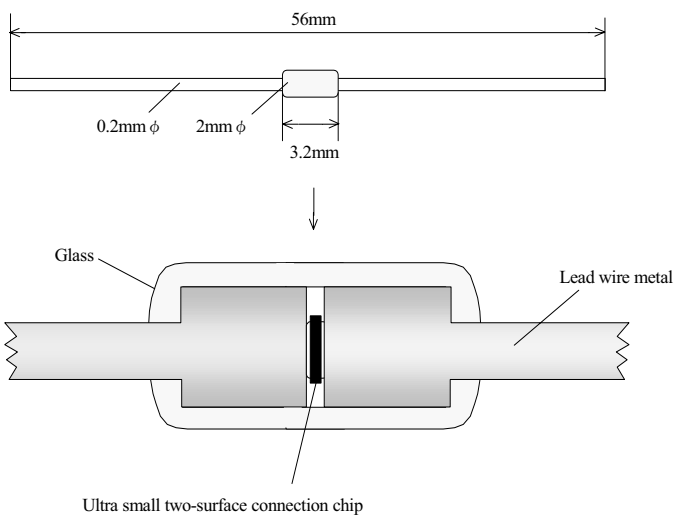

Figure 22.7.5: Ultra small chip in glass encapsulated package.

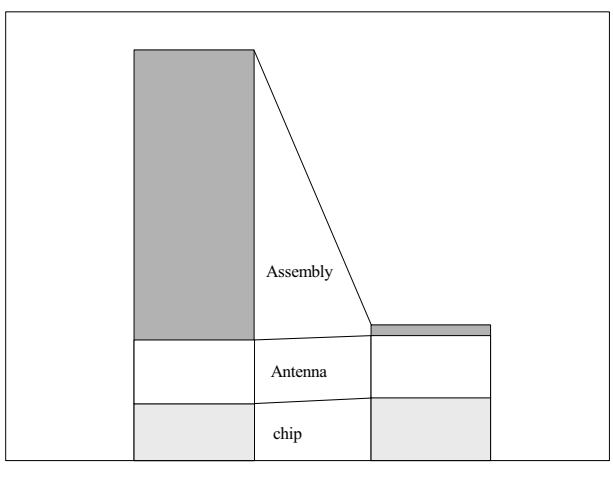

Figure 22.7.6: RFID inlet cost comparison.

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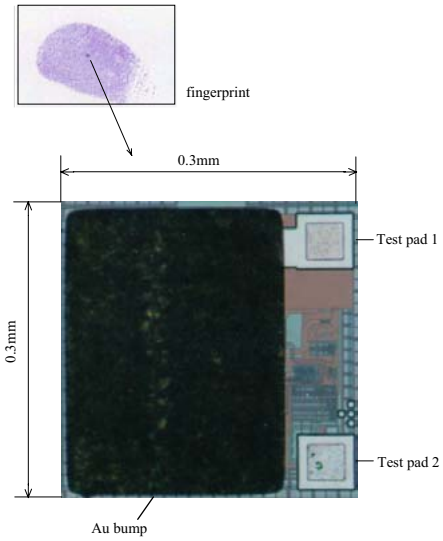

Figure 22.7.7: Photomicrograph of the developed chip.

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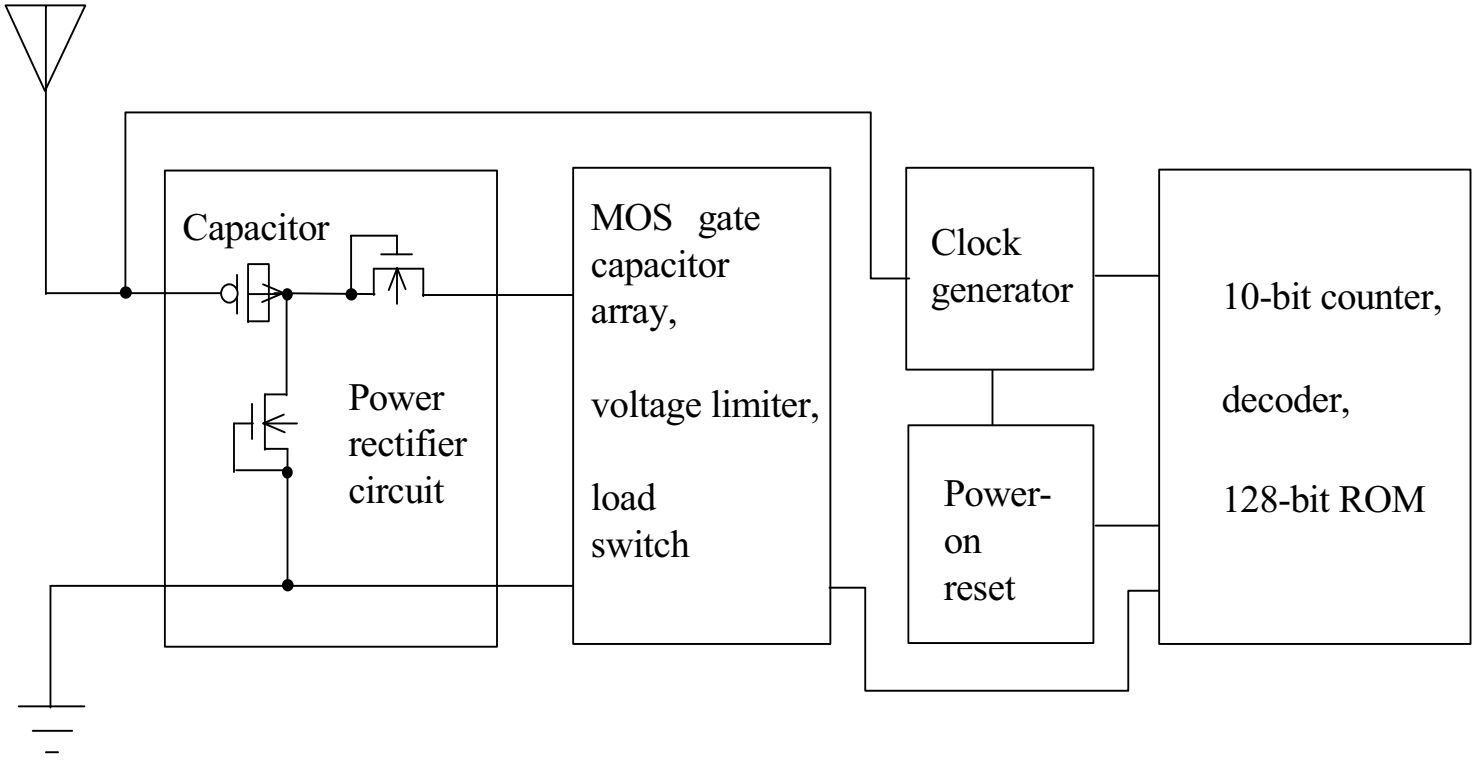

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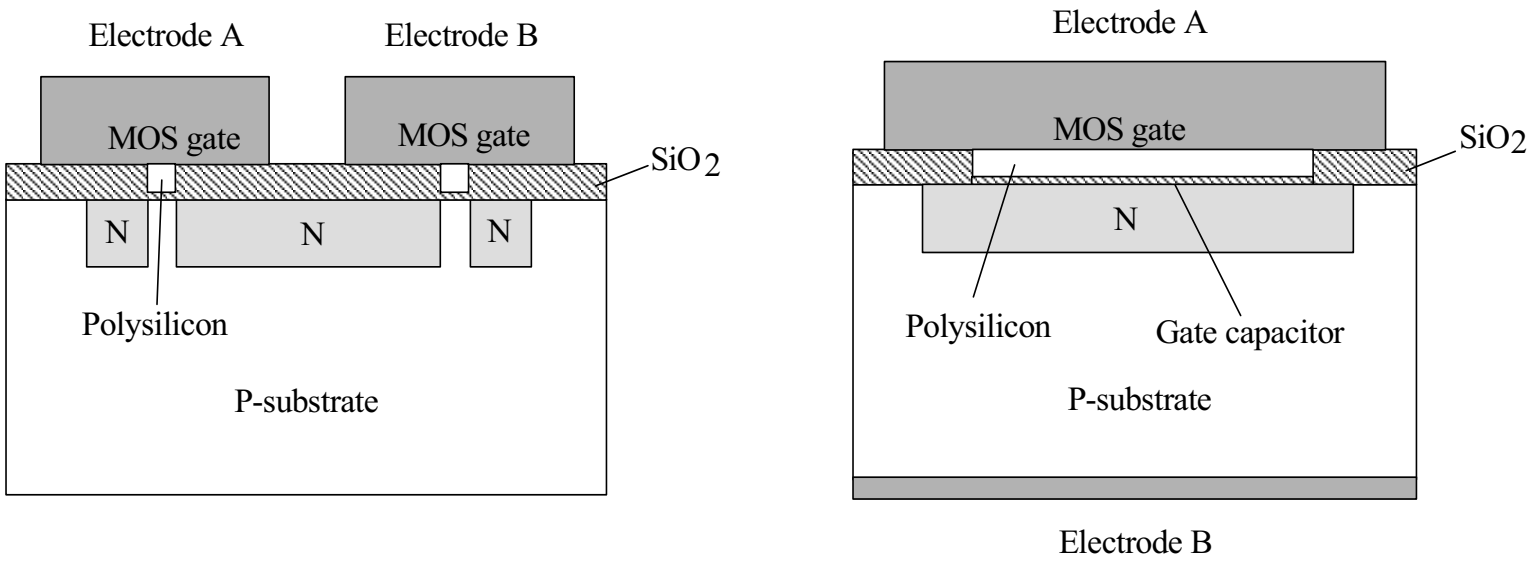


Figure 22.7.2: Simplified input device structure comparison.

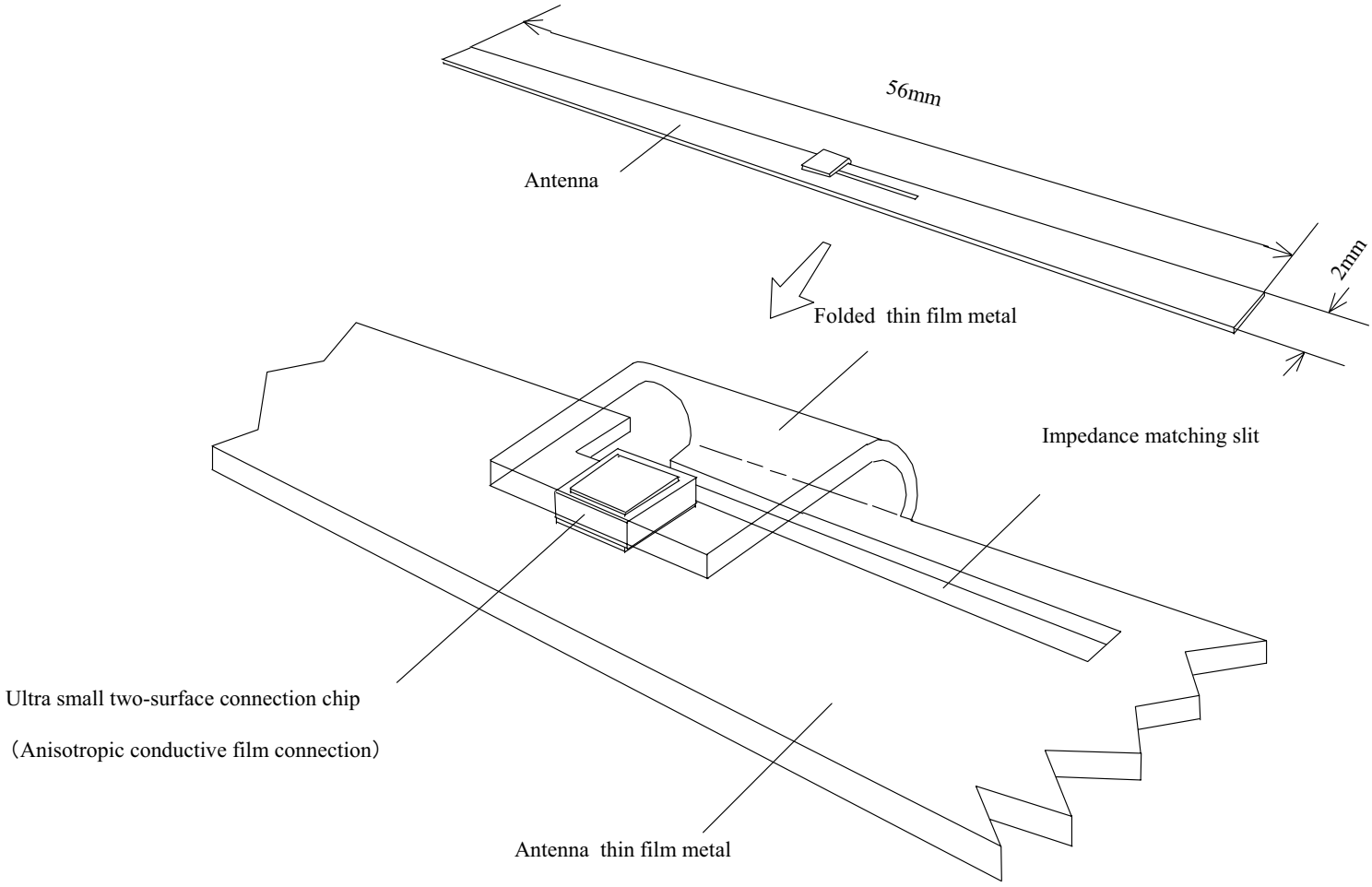
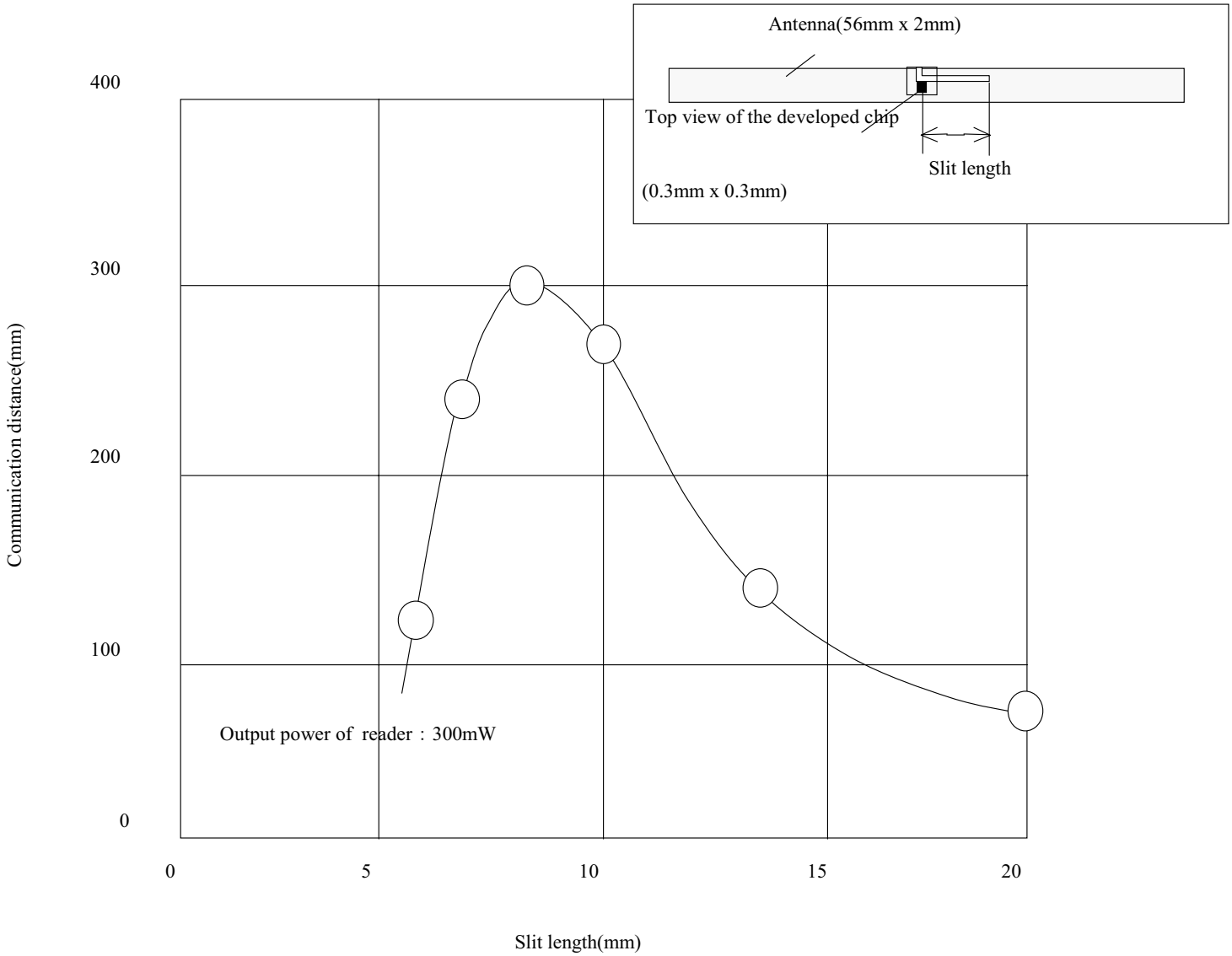


Figure 22.7.3: Connection structure of two-surface connection chip.



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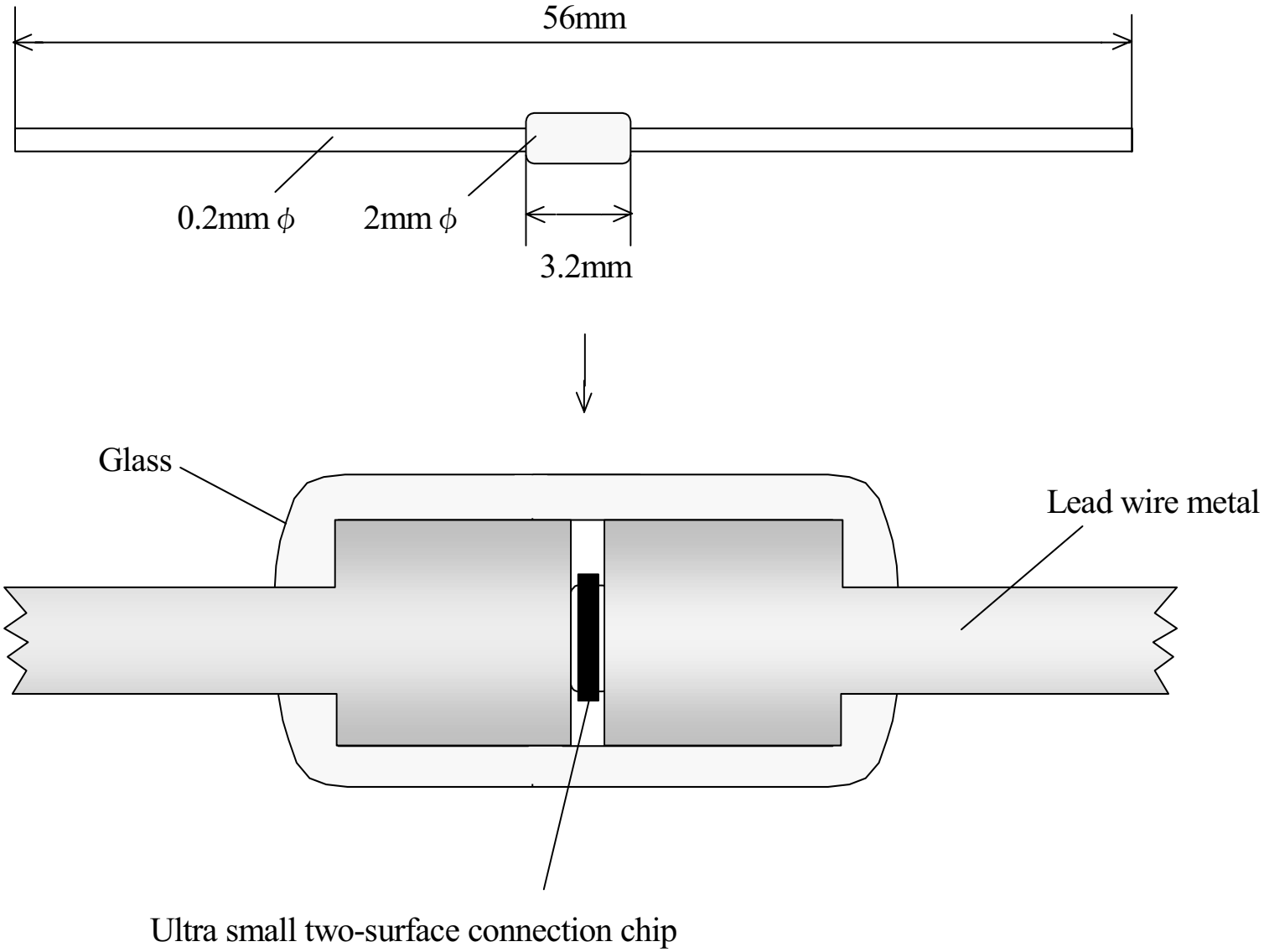

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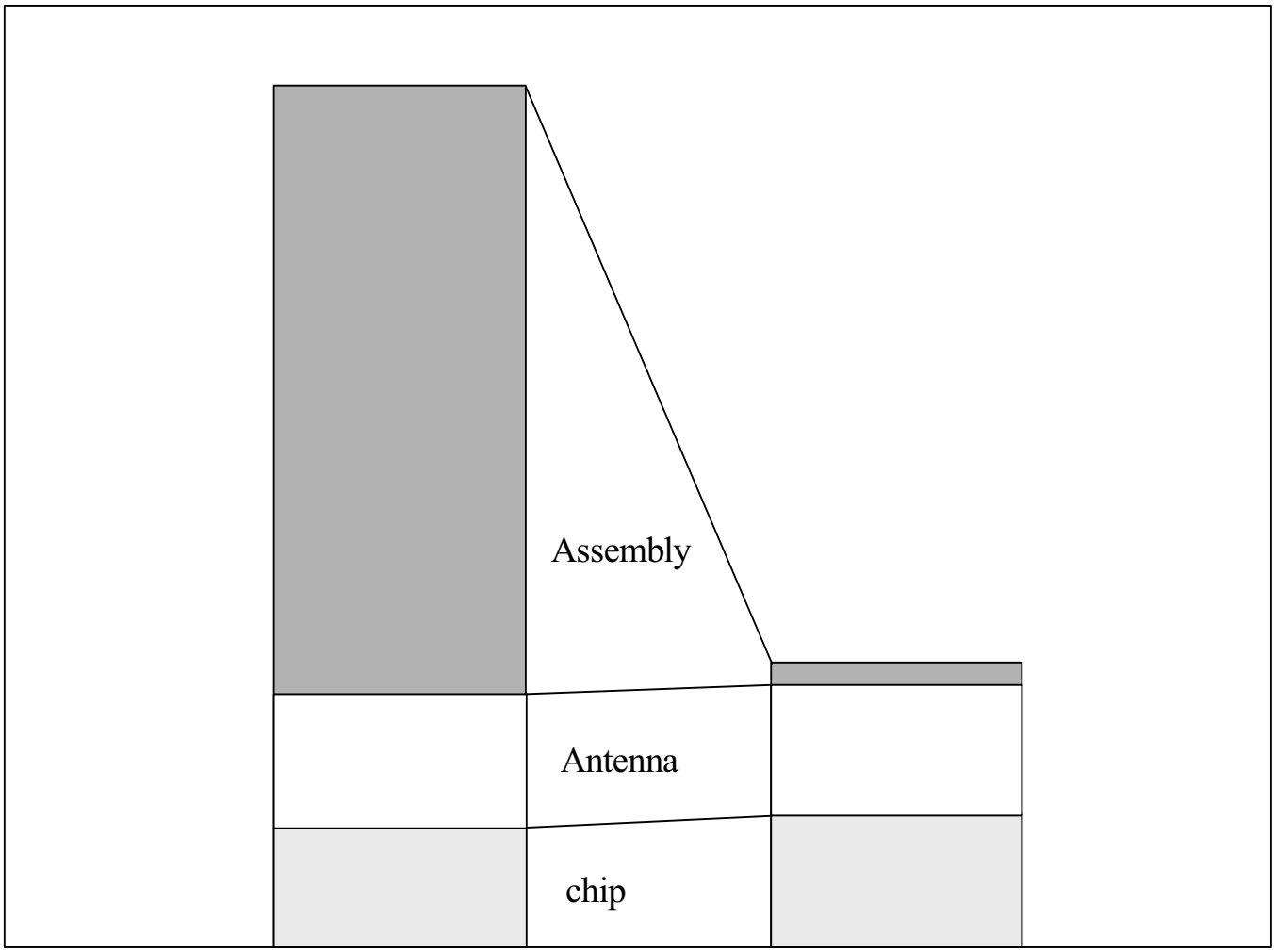
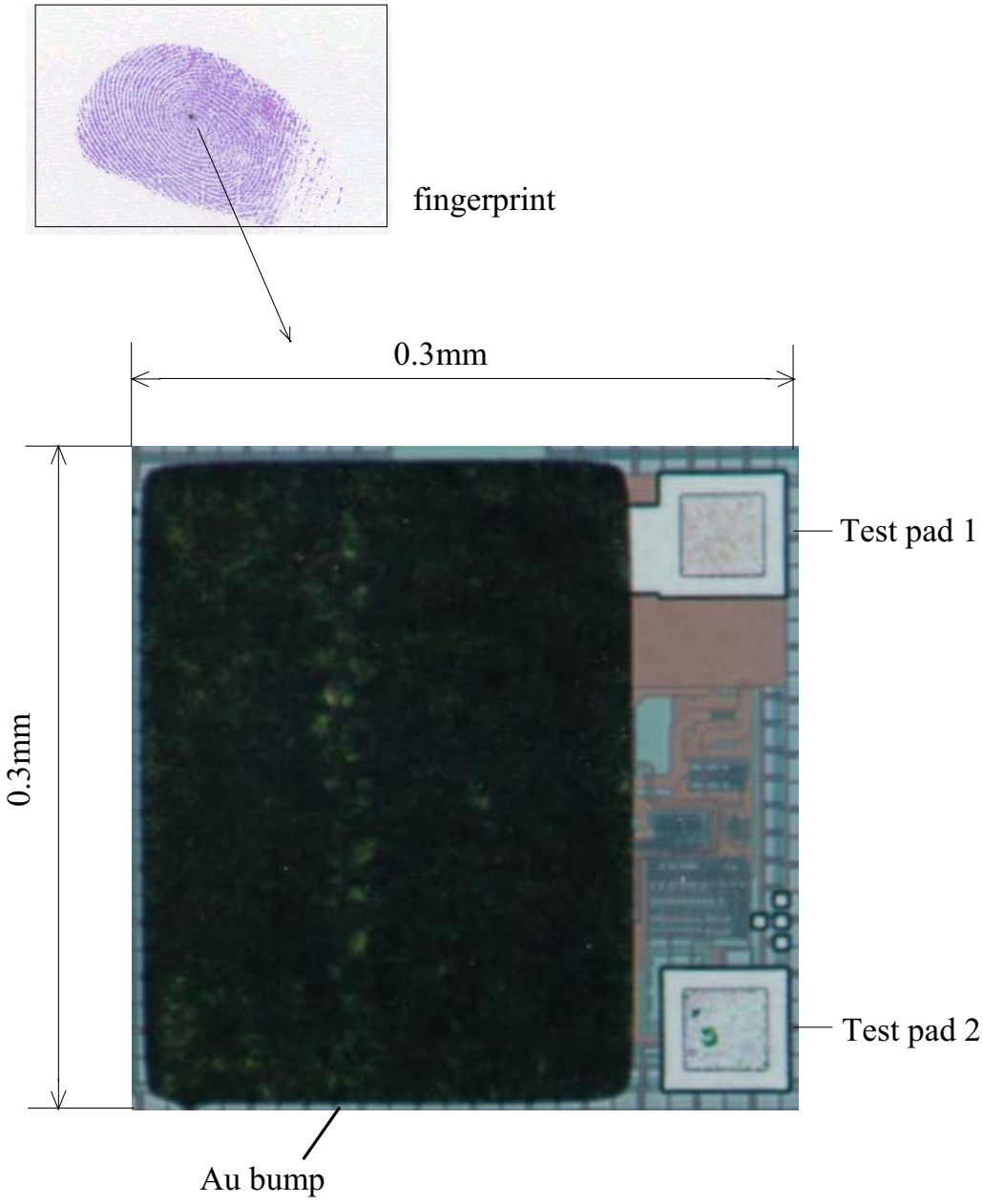


Conventional: Single-Surface Connection **New Chip: Two-Surface Connection**

Figure 22.7.6: RFID inlet cost comparison.



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