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Architecture of a μRFID with integrated antenna in 3D SOI-CMOS

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***Abstract*— We report on an implementation of a self-powered radio-frequency identification tag in a three-dimensional silicon on insulator (3D SOI) process, which uses backscatter modulation to send a hardwired digital code to a scanner.**

I. Introduction

Wireless communication and power is extremely valuable for many applications, [2]. This involves building a hybrid system incorporating both RF design and digital logic, a challenging task in any process. The new experimental three-dimensional silicon-on-insulator (3D SOI) technology, where three chips are bonded together and communicate via inter-connects, would be particularly advantageous in this situation, as one could conceive of combining a chip fabricated in an RF process with another chip from a low-power digital process, each chip optimised for its function within the overall system. This is especially true when one considers the design of uRFID systems with integral antennas designed to operate in the 24Ghz frequency range.

The experimental nature of the process encourages a simple system as a first step, to demonstrate the ability to gather power from the environment, use that power to generate a signal, and transmit the signal back to a receiver. All of these elements are present and comparatively simple to implement in an radio-frequency identification (RFID) tag system.[2]

RFID systems are designed to consume very low power[3] and occupy very small area.[5] Both of these conditions result from the desire to make the system as small as possible, to give the RFID tag the widest possible range of applications. The power requirements must be small to make the antenna small as the biggest factor in determining the size of the system is the external antenna. In fact, the actual chip area contributes very little to the overall system size.[4] Packaging the external antenna onto the chip is also non-trivial.

The systems implemented in this paper use on-chip antennae and backscatter modulation to collect power from a RF source and communicate a unique, hardwired signature back to a detector in a scanner. The chip itself is comprised of 3 stacked chips, with inter-tier vias providing communication between the different tiers. The space constraint is such that the entire top tier was filled with pads to probe test structures, three versions of circuits are implemented in the middle tier (two whole systems and one broken up into test constituents) and all of the antennae are on the bottom tier. Thus, a full system

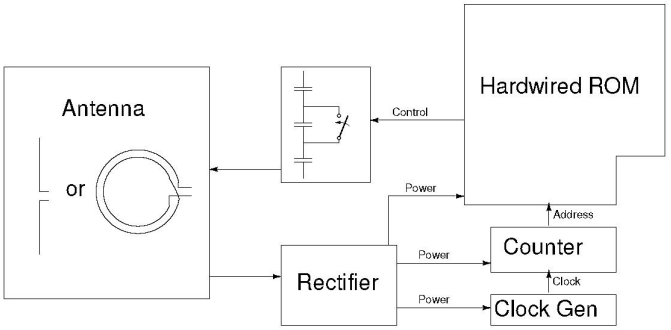

Fig. 1. Overall block diagram of the RFID system

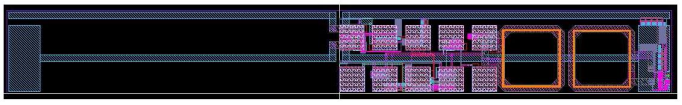

Fig. 2. Layout of the entire system, all 3 tiers

is comprised of the antenna on the bottom tier and all of the circuitry within a very small area on the middle tier (see figure 6). The small size of the antennae necessitates working at frequencies in the tens of gigaHertz, to maximise the amount of power collected for such a small area.

II. Antennae

The 3D chip is only 3 mm to a side, and for this application a thin 2mm long sliver was allocated. Hence dipole antennae 2 mm long on the bottom tier are separate from circuits in the middle tier. Also included are two large 200 μm diameter coils to test if the circuits would perform better in a transformer-style mode. One each of the dipole antennae and the coil are wired to two full implementations of the circuit; the remaining dipole and coil are wired to test structures. For the dipole attached to the full circuit, two dumbbell-style lobes at the ends are added to increase the effective length of the antenna, thus reducing the necessary frequencies that the system must operate at.

Simple calculations show that for a 2 mm $\lambda/2$ antenna implies an optimal wavelength of 4 mm or a frequency of 75 GHz. However, the system should be capable of operation at frequencies in the mid 20 or 30 Ghz if the transmitter is in close proximity to the RFID.

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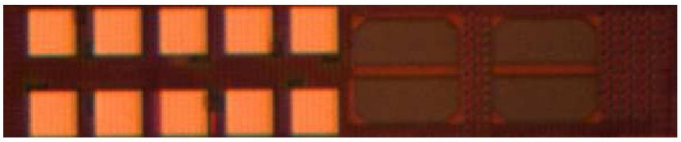

Fig. 3. Micrograph of the entire system, top view. Note the pads and the antennae, the two large coils and half of the dipole. The remainder is obscured by fill.

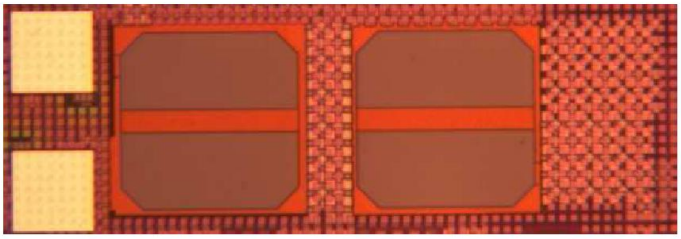

Fig. 4. Close-up of the coils

III. Backscatter modulation

If the receiving antenna is not perfectly impedance matched to its surroundings, part of the incident RF waves will be reflected back to the surroundings. This reflected wave can be detected, and can be modulated according to the impedance characteristics of the antenna. The load of the antenna is modulated digitally with a distinct digital signature, such that when the scanner sends the input wave, the reflected wave has this digital signature and the presence of this RFID tag can be detected.

This was achieved by adding a variable capacitance across the antenna. This capacitance is made up of three capacitors in series (two of which are 500 fF and one is 250 fF). Capacitors in series add like resistors in parallel, thus the smallest element make up the greatest contribution to the overall capacitance as seen from the antenna. By shorting out the smallest capacitor with a single MOSFET as a switch, this then gives the biggest capacitance change which then should result in a discernible change in the backscattered signal.

IV. Power rectification

The power rectifier is a 2 stage charge pump[6] that leads to an effective doubling of the input voltage, subtracting losses due to diodes. A limiter comprised of two diodes in series at the output prevents the voltage from rising too high.

The diodes are PMOS SOI diode-connected transistors; the ones in the rectifier are 8 μm width and 200 nm length,

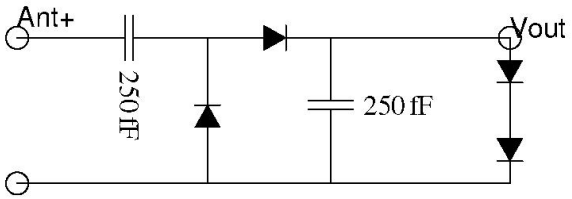

Fig. 5. Rectifier schematic

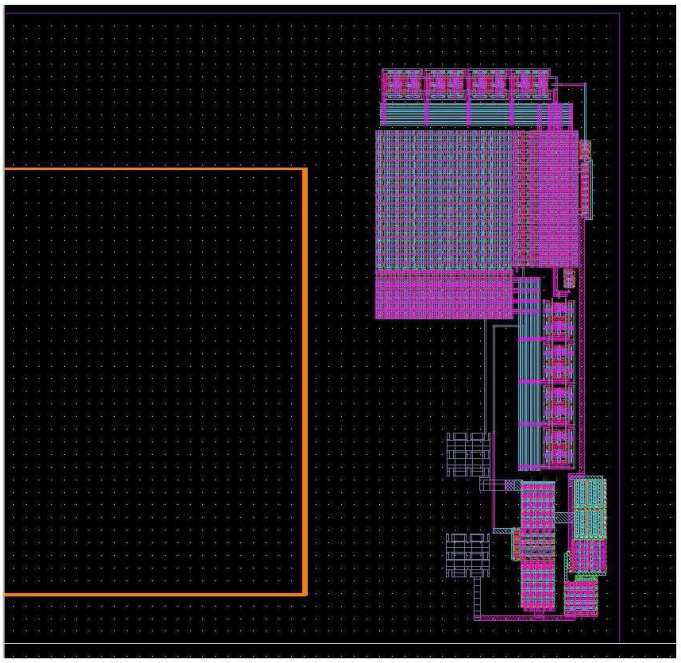

Fig. 6. Middle tier closeup of right-hand side, with a full RFID system. The "do not fill" box on the left is over the coils and is 200 μm to a side. The hardwired array is at the top, with decoders. The rectification circuit and the modulator are bottom right and left respectively. Note also the large inter-tier via arrays to connect to the bottom layer antenna, in this case a coil on the left.

while the limiters are 120 μm width and 200 nm length. The limiters prevent the voltage from rising above 1.2 V, and given an incident power with a frequency in the tens of GHz the supplied voltage is expected to be no less than 0.7 V, according to simulation.

V. Digital Control

The supplied voltage is used to generate a digital signal to modulate the load for backscatter. A simple ring oscillator generates a clock signal in the tens of MHz, which is a much easier frequency range in which to design subsequent circuits in. This clock signal clocks a series of D flip-flops arranged in toggle configuration to work as a counter, with undetermined initial state. This is of no consequence for it avoids the necessity of generating a synchronization signal between the tag and the receiver, so this architecture simply cycles through each of the states in order, and the receiver will then need to detect a full sequence of all of the states in order to identify the tag.

Using these storage elements an array of hardwired elements is addressed, such the each row or column codes a digital "1" or "0". This signal is then used to modulate the backscatter modulator.

Due to area constraints this is implemented with two 4-bit registers that then address an array of 256 elements. The entire array is laid out automatically using Skil code and eight small building blocks, making expansion of the array a simple exercise in modifying the function arguments. The code is

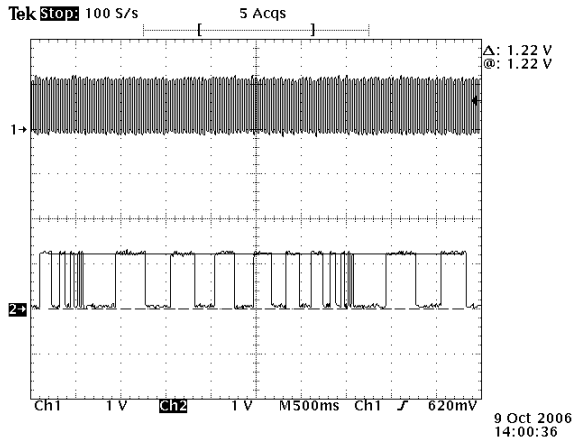

Fig. 7. Oscilloscope plot of output with 75 Hz input clock; Note the decreasing number of highs and lows with increasing time. Also note the cycle repeats continuously.

designed so that any arbitrary sequence of 1's and 0's could be implemented; for ease of testing a series of primes is used in this case, such that the first n zeroes is followed by n ones, and then m zeroes and m ones, where n and m are consecutive prime numbers. This sequence is monotonically increasing and fairly distinct, making it easy to look for and ideal as a test case. The argument used to generate the signature array is shown below, using the bottom right corner as the starting point, and going right to left before going up in the array. This is done in this manner to make connection of other elements in the layout simpler.

```
array=vector(
  vector(1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1)
  vector(1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0)
  vector(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
  vector(0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1)
  vector(1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0)
  vector(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
  vector(0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1)
  vector(1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0)
  vector(0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1)
  vector(1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0)
  vector(0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1)
  vector(1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0)
  vector(0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1)
  vector(1 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1)
  vector(1 1 1 0 0 0 0 0 0 0 1 1 1 1 1 0)
  vector(0 0 0 0 1 1 1 0 0 0 1 1 0 0 1 0)
  );end array
```

A board custom-designed to test this chip clocks the array at a slow rate (approximately 10 Hz) and obtains the output value through a serial interface. This is controlled in turn by a Matlab program that automates the data collection process.

This is the sequence of ones and zeroes obtained repeatably from 1000 clock cycles at 10 Hz, with the zeroes in the left column and the ones in the right column:

```
data01 =
     2     5
     5     7
     7    11
    11    13
    13    18
    17    19
    19    23
    23    27
    26     1
     1     2
     2     3
     3     5
     5     7
     7    11
    11    13
    13    18
    17    19
    19    23
    23    27
    24     0
```

There are two obvious discrepancies with the specifications as given above. Firstly, it appears that the digital ones lead the digital zeroes, with 5 ones preceding the 5 zeroes, and then 7 ones followed by 7 zeroes and so on. This can be attributed to having an uneven number of inverters in the pad driver chain, thus turning all of the digital ones to zeroes and vice versa.

The other is that the numbers do not appear to be prime. The start and the end may be discounted, as these counts are truncated due to the time the observation begins being random relative to the starting point of the array, for reasons mentioned above. This leaves an 18 in the ones column. In addition, a 26 and 27 count are observed in the zeroes and ones column respectively. None of those numbers are prime numbers.

However, careful inspection of the array description above shows there actually is a sequence of 18 zeroes in the middle, and a sequence of 26 ones and 27 zeroes at the very top. When the inversion as described above is accounted for, this is clearly the signature of the hardwired array as specified. Any discrepancies between the output and the intended prime sequence are due to errors in the design of the array!

Operating this setup at 2 MHz yields a large number of glitches on the output, leading to erroneous, non-repeatable sequences collected by Matlab that increase monotonically but do not correspond in general to the signature above.

Finally, it may be noted that the count according to the scope (Figure 7) is monotonically decreasing, whilst this data shows an increasing trend. The decreasing trend is due to miswiring of the polarity of the array, such that it will count from the top left corner to the bottom right. The data is collected using a recursive update subroutine which saves the oldest data at the bottom of the array, and pushes the newer values onto the top,

in a stack-style storage structure. Hence the data appears to match the polarity of the originally intended array, whereas in fact the opposite is true. This only reinforces the notion that a signature designed in this fashion aids the testing process immensely in observing trends in the output data that can assist in determining functionality of the system.

VI. Conclusions

The complete RFID tag has been implemented in a 3D SOI process. The low frequency digital structures have been tested and shown to produce a signature identical to the hardwired signature which is necessary to identify the tag. These digital structures do not appear to function correctly at the higher frequencies intended for normal operation. Further testing is needed to properly evaluate the higher frequency non-digital components of the system as well as the system in its entirety. A version of these circuits is in fabrication in an updated process to facilitate testing of the structures described above.

VII. Acknowledgements

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