Experimental results of simplicial CNN digital pixel processor

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Experimental results of an integrated circuit implementing a simplicial cellular nonlinear network digital pixel processor are presented. The prototype has a 7 × 6 cells array, and works as expected at a testing clock speed of 10 MHz.

Introduction: This Letter presents experimental results of an integrated circuit prototype implementing a simplicial cellular nonlinear network (S-CNN), the circuit architecture and behaviour of which have already been described in [1]. Several CNN realisations have been reported in the literature [2–4], but the operation of most of them is based on the standard CNN [5], which is characterised by a state difference/differential equation that is linear on inputs and states. This provides a relatively simple circuit realisation, at the cost of loss of generality. On the other hand, the state difference/differential equation of an S-CNN uses a simplicial piecewise linear (PWL) algorithm, originally proposed in [6]. As a result, the S-CNN is more general, and can be used to implement more complex algorithms in a more direct way [1]. The chip described in this Letter is completely digital, albeit the photodiode and its interface. To achieve a small pixel size, the S-CNN cell parameters are moved out of the cell into a unique memory, outside the array, and broadcast to every cell.

Circuit description: The array has 42 cells (7 × 6) arranged in a hexagonal pattern (Fig. 1 shows the distribution of cells, and the internal blocks of one cell with the internal signals and buses). Accordingly, every cell has seven neighbour cells (including itself). As described in [1], the S-CNN algorithm requires the following stages. First, the cell input u_i needs to be converted to a 7-bit digital word. This is done by measuring light intensity with a reverse-biased diode, and the analogue to-digital conversion is done using a single ramp conversion with an analogue ramp and an analogue comparator common to all cells.

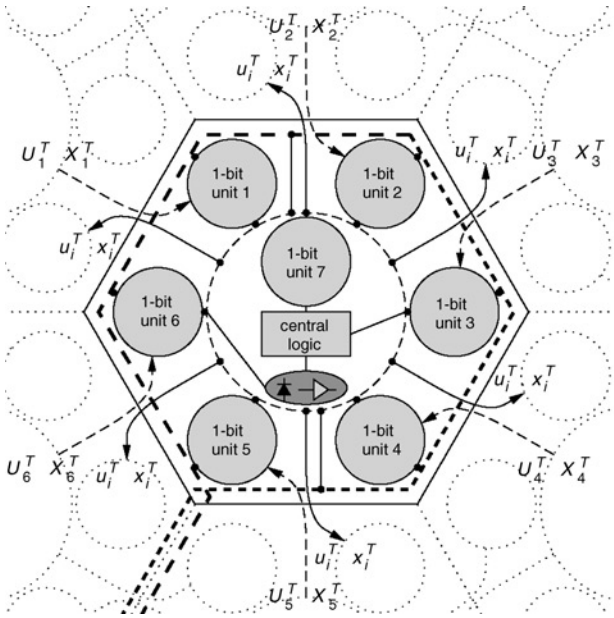

Fig. 1 *Schematics of unit cell and comparator*

Secondly, input u_i and state x_i (also a 7-bit word) need to be compared to a 7-bit digital ramp during a cycle, called program cycle (PC) of $2^7 = 128$ steps. This comparison is done by an XOR gate, implemented bit by bit using precharge-evaluate dynamic logic (see Fig. 2). The resulting signals are two 1-bit signals (u_i^T, x_i^T) that have the information of the cell input and state, respectively, coded in time. These signals, and the equivalent signals belonging to the six neighbours, are arranged to form 7-bit time-coded words (u_i^T, x_i^T). These words are used to address the memory and retrieve the parameter values, which are the values of the logic function to be implemented by the SCNN, $G(U_i^T)$ and $F(X_i^T)$, respectively. As the memory is outside the cell, this is done as follows. For every single step of the PC, a digital ramp and the values of the memory are distributed to all cells through the bus, and compared in every cell with the 7-bits time-coded word. When there is a coincidence (the dynamic XOR comparator is re-used to do this), the memory value is latched in a register. This internal cycle is called the memory evaluation cycle (MEC). At every step of the PC, the value retrieved from the memory (one-bit) needs to be added by a counter, which at the end of the PC will update the state. Actually, the counter has been implemented indirectly in the following way. At the end of the PC, if the count (stored in a register) needs to be increased by one, a flag is set, and in the next MEC an equality comparator (implemented re-using the dynamic comparators) detects when the ramp is equal to the current count, and stores the next value of the ramp, therefore increasing the register value by one. This eliminates the need for a counter, and can be done very efficiently using an equality comparator. As can be seen from Fig. 1, all comparator, latch and register circuits are spatially distributed within the cell, so that the connection to neighbour cells is optimal in terms of layout.

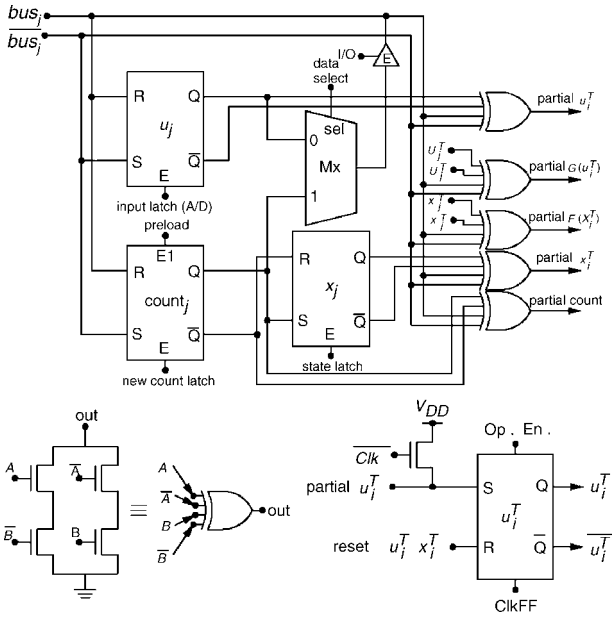

Fig. 2 *Cell architecture*

The IC was integrated in an *n*-well non-silicide CMOS process of 0.5 μm AMI through the service provided by MOSIS, in an area of 3 × 3 mm. This process has three metal layers and two poly layers (one metal layer was completely used for light masking). A picture of the IC is shown in Fig. 3

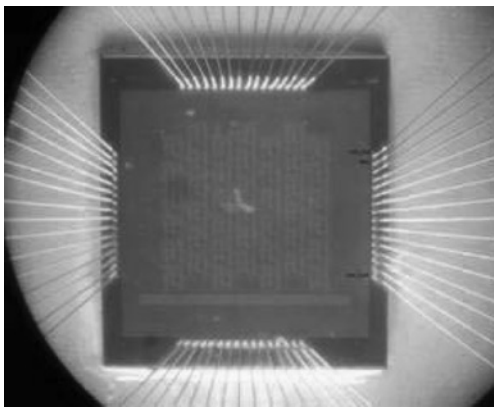

Fig. 3 *Die photograph*

Test results: The IC was tested using two boards. One of them allocates the IC and the other is a multipurpose board (MPB) with a serial interface (MAX233), one PIC (18LF6680), two CPLD (XC2C32A), and D/A converters (DACLTC 1660). The board is responsible for the generation of all control and data signals and also for reading the values

produced by the IC. The PIC sets the operating frequency of the SCNN chip to 10 MHz. Once the light acquisition stage and the individual parts proved to be correct, the chip was programmed to acquire an image and implement different functions.

Fig. 4 shows an original image and the results of the right-down, down, twice-down translation functions. Fig. 5 shows an original image, and the results of the erosion, edge detection and inversion functions.

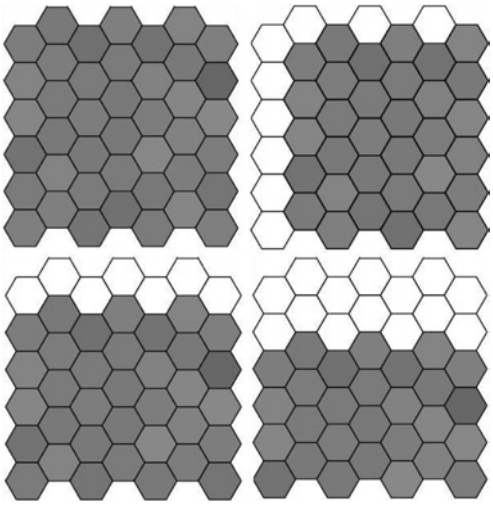

Fig. 4 *Translations applied to input image*

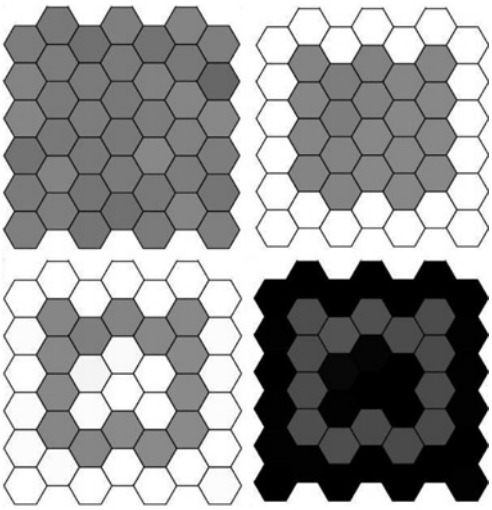

Fig. 5 *Erosion, edge detection and inversion applied to input image*

Conclusion: The first operating prototype of an S-CNN image processor has been demonstrated. A 7 x 6 cells array was built in a 0.5 μm process, in an area of 3 × 3 mm. The IC was successfully verified with several logic functions at a clock speed of 10 MHz.

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