Lab:#1 MOS Transistors I-V characteristics and Model Parameter Extraction

March 3, 2017

The objectives of the first lab are:

1. To become acquainted to CD4007 MOS transistor array.
2. To obtain the I-V characteristics of both P type and N type devices.
3. To perform measurements on your devices, and determine SPICE simulation parameters.
4. Use SPICE to obtain the I-V characteristics of the transistors and compare with those obtained experimentally.
5. Learn how to use the library and the scientific literature.

1 References

1. Modeling and simulation of insulated-gate field-effect transistor switching circuits [1]
2. SPICE program manual
3. Analysis of oscillatory metastable operation of an RS flip-flop [2]
4. CD4007A CMOS Dual Complementary Pair Plus Inverter, Texas Instruments reference manual, pp. 3-14 to 3-17.

2 Warning!

Please follow all the anti-static procedures when handling the CD4007 CMOS devices.

3 Introduction

Computer Aided Design tools such as SPICE and Microwind are used today by engineers and to create virtual prototypes and simulate their circuits. Their accuracy in simulating complex circuits will depend on the models used and on the parameters that are given in its models. In the class we discussed MOS transistor models and how they depend on model parameters. In this lab, we will become familiar with extracting experimentally model parameters for the devices found in the CD4007 integrated circuit that includes MOS transistors (P-type and N-type). This integrated circuit is the same as an earlier integrated circuit produced by RCA the CA3600 MOS transistor array.

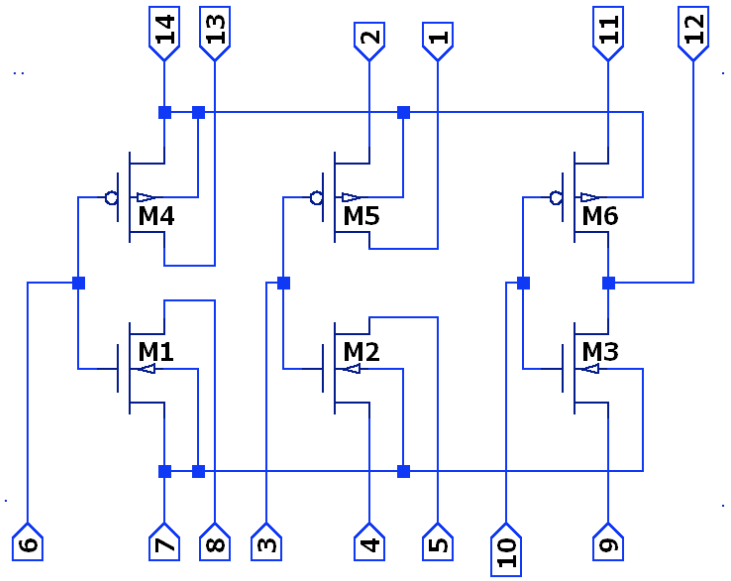

Figure 1: Internal schematic diagram of CD4007 integrated circuit.

4 The CD4007 MOS integrated circuit

The integrated circuits to be used for this week experiments are made by Texas Instruments. This is one of only a handful commercially available integrated circuit with discrete MOS transistors; three P-type and three N-type. Figure 1 shows the way these transistors are connected internally and to the pins of the package. Note that because there are not enough pins on a 14-pin DIP package, some terminals from different transistors are connected together and they come out of the package, on a single pin. **Be aware of these internal connections when using the devices to build your circuits!**.

5 Experiment 1: I-V characteristics of a resistor

Familiarize yourself with the instrument for measuring current, and the variable power supplies in the lab. Prepare three cables (red and black) with "banana" plugs at the ends and

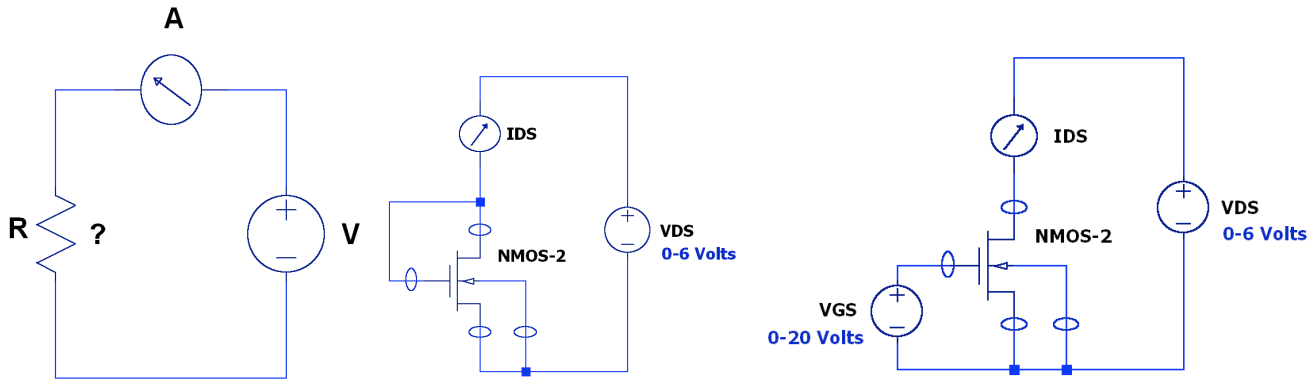

Figure 2: Experimental setups. Resistor I-V characteristics (left), NMOS transistor I-V characteristics saturation (middle), NMOS transistor I-V characteristics linear-ohmic (right).

about 1 meter long, enough to reach from the instruments on top of the bench to your bread-board. Connect the mystery resistor as shown in the circuit Figure 2(left) and measure the current through the resistor for 5 different voltages V. Plot the results in Excel or any other program that you want to use and confirm that the device that you measure is a resistor. Estimate its value.

6 Experiment 2: I-V characteristics of N-type MOS devices

Use a bread-board to place your CA4007UB integrated circuits. When you are finished, connect all of the gates of the transistors to pin 7. Do not remove the device from the bread-board.

6.1 Saturation region

Connect the gate of the transistor to the drain and your ammeter to obtain the I-V characteristics the I-V characteristics for an N-type transistor (Pair 2 on the chip) with the devices working in the saturation region Figure 2(middle). Why is the device now guaranteed to be in the saturation region? Perform the experiment just once with $V_{BS} = 0$. Take measurements for currents up to 10mA at $V_{DS} = 0$, 0.2, 0.4, 0.8,1.6, 3.2, 6.4, 12.8

6.2 Linear/ohmic region

Use the circuit shown in Figure 2(right) to obtain and plot the I-V characteristics for an N-type transistor (Pair 2 on the chip). For all these measurements in the linear region, set $V_{DS} = 0.250V$. This can Determine the I_D versus V_{GS} characteristics for $\mid V_{GS} \mid$ values between .250, 0.5, 1, 2, 4, 8 and 16 Volts. Note that for the N-type devices V_{GS} is always > 0. Use the HP instrument as an ammeter for these measurements and the variable voltage power supplies in the lab for the variable voltage sources.

In the write-up, show the circuits you have used and include the arrows on the substrate contact of the transistor as well as the polarities of the voltage sources.

7 Post-lab Analysis: SPICE parameters extraction

7.1 Linear region

The equations of the LEVEL 1 model were given in the class. (We are justified using the LEVEL 1 model because our devices are large (both the width and the length of the channel). Under the experimental conditions used for obtaining the data, the current I_{DS} can be rewritten as: (Why?)

$$I_{DS} = \beta(V_{GS} - V_{TH})V_{DS} \tag{1}$$

where

$$\beta = KP\frac{W}{L} \tag{2}$$

Use the I_{DS} versus V_{GS} plots and the equations above to determine the extrinsic transconductance parameter β, and V_{TH} for the three different V_{BS} values. From β you can find KP, given that for the devices used $W_P = 580\mu m$, $W_N = 300\mu m$ and $L_{P,N} = 20\mu m$. The threshold value determined at $V_{BS} = 0$ is the VTO parameter in SPICE.

7.2 Saturation region

As an alternative to the previous method, it is possible to measure the same parameters in the saturation region. The equation for the drain current in the saturation region is given by:

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \tag{3}$$

This suggests that if you plot $\sqrt{I_{DS}}$ versus V_{GS} you can determine β and V_{TH}. Do that!

8 Extra Credit

8.1 Reverse engineering the die

The length and the width of the transistors were determined by *reverse engineering* from the microphotograph of the CA4007UB die shown in page 4 of reference 4. I believe that the figures I gave you are correct. 1) Identify the 6 transistors on the die and color them. Hint: The die shows top level metal and the numbers in the squares at the periphery of the die correspond to the bonding pads. 2) Verify that the dimensions of the transistors are more or less what I have given you above.

9 Lab Report

1. Describe the basic experimental setup and procedures for the experiments. Show the measurement results in tables. Show the diagrams in Figure 2 but mark the chip pins in the circles at the terminal of the transistors.

2. Show your work results for the parameters extraction.

3. Discuss the results of your experimental work.

References

[1] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," *IEEE Journal of Solid-State Circuits*, 1968.

[2] T. Kacprzak, "Analysis of oscillatory metastable operation of an RS flip-flop," *IEEE Journal of Solid-State Circuits*, 1988.