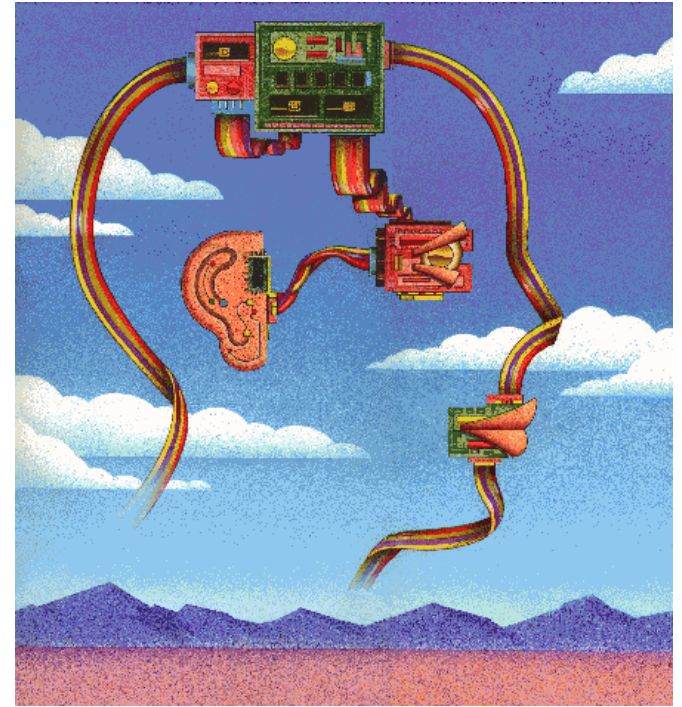


Making a Chip that Sees

a.k.a. Introduction to VLSI Systems



Andreas G. Andreou

andreou@jhu.edu

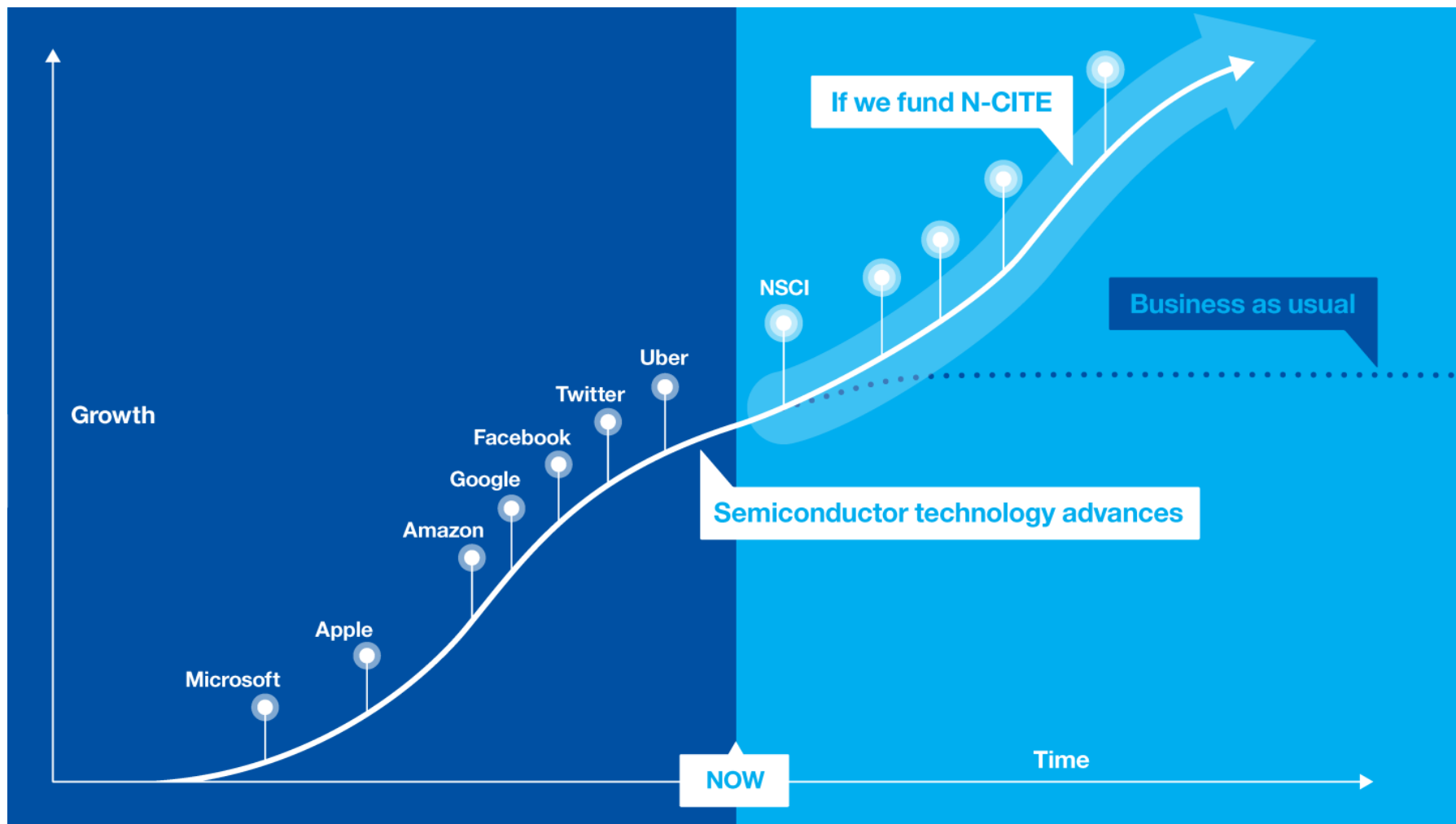
Electrical and Computer Engineering

Center for Language and Speech Processing

Johns Hopkins University

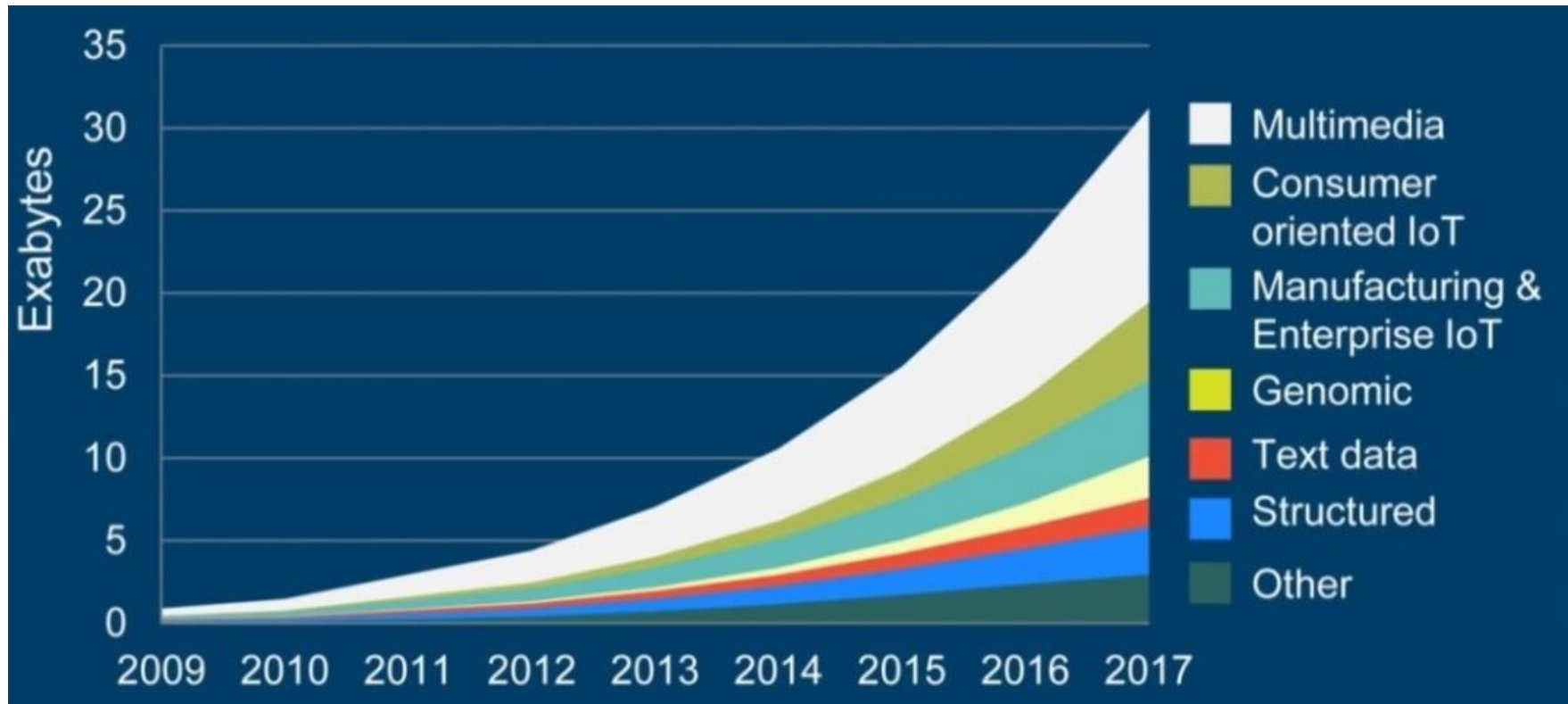
<http://www.ece.jhu.edu/faculty/andreou/AGA/index.htm>

economic growth depends on chips

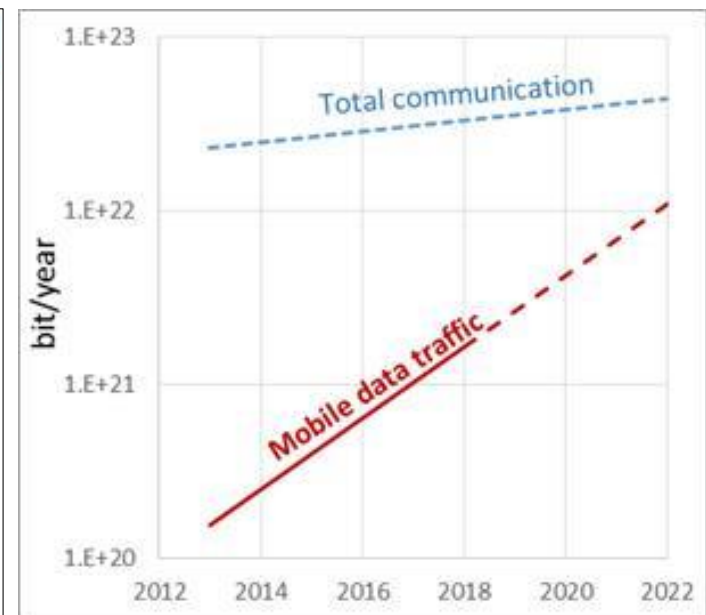
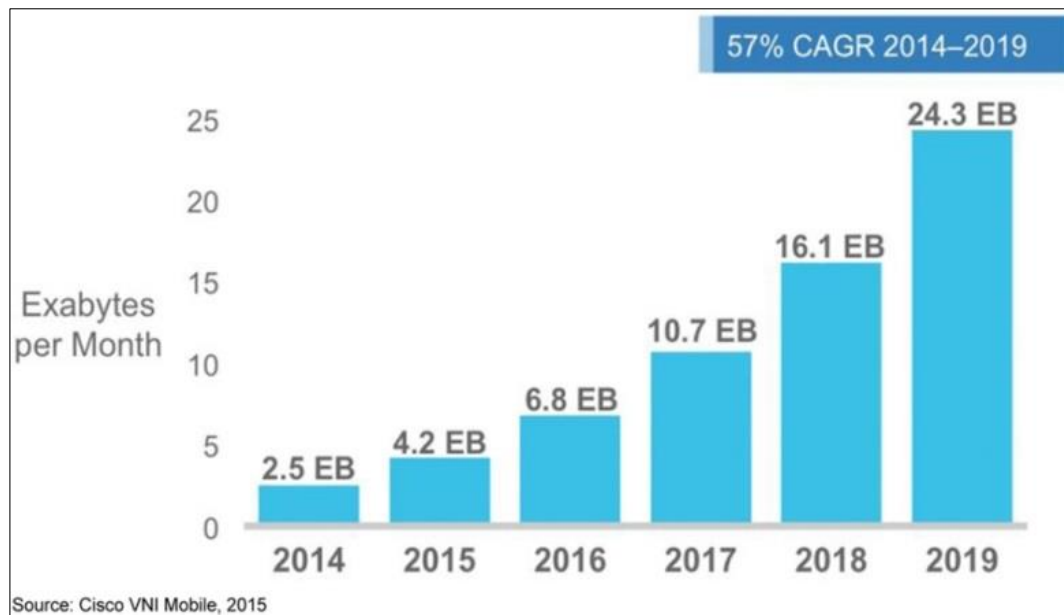


Rebooting the IT Revolution: A Call to Action, SRC, Sept 2015

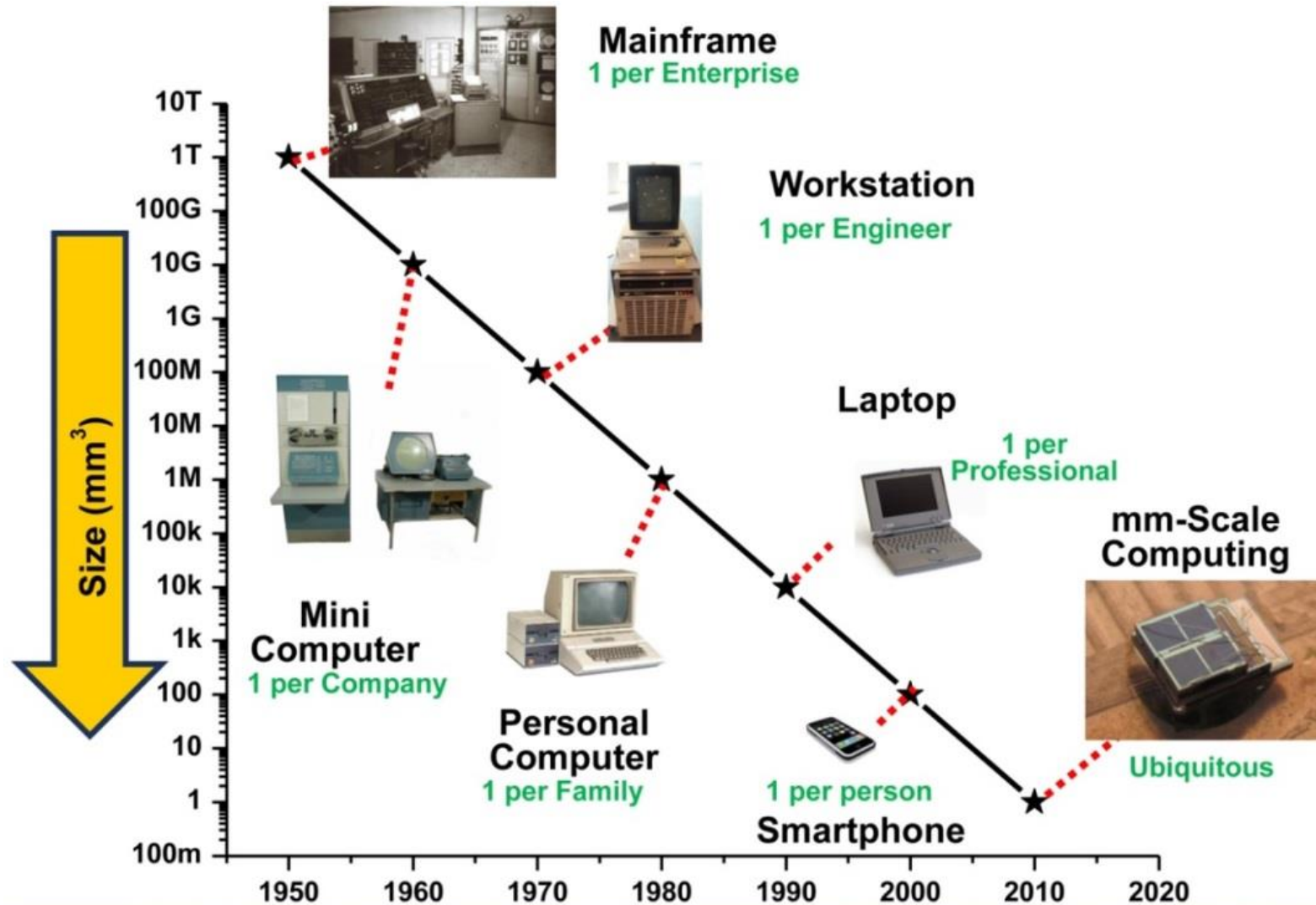
BigData growth



mobile data growth



computer size



Rebooting the IT Revolution: A Call to Action, SRC, Sept 2015

computers and the brain

Mammalian Brains vs Computers

Parallel distributed architecture

Low power (25W), small footprint (1 liter)

Asynchronous (no global clock)

Analog computing, Digital communication

Integrated memory and Computation

Intelligence via Learning thru BBE interactions

Composed of noisy components and operates at low speeds (< 10 Hz)

Spontaneously active



Serial architecture

High power (100MW), Large footprint (40M liters)

Synchronous (global clock)

Digital computing and communication

Memory and Computation are clearly separated

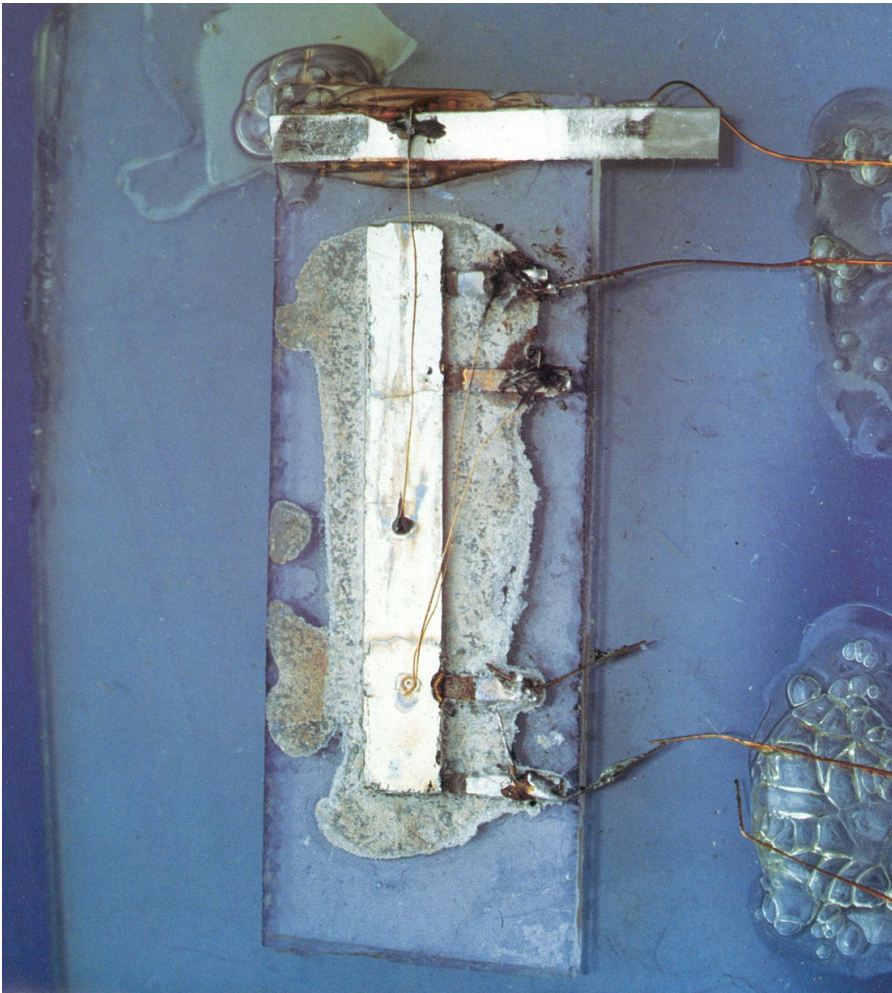
Intelligence via programmed algorithms/rules

Precision in components and operates at very high speeds (GHz)

No activity unless instructed

Back in the 50s

Jack Kilby, Texas Instruments,
Phase Shift Oscillator (1958)



The Nobel Prize in Physics 2000



Zhores I. Alferov
Prize share: 1/4



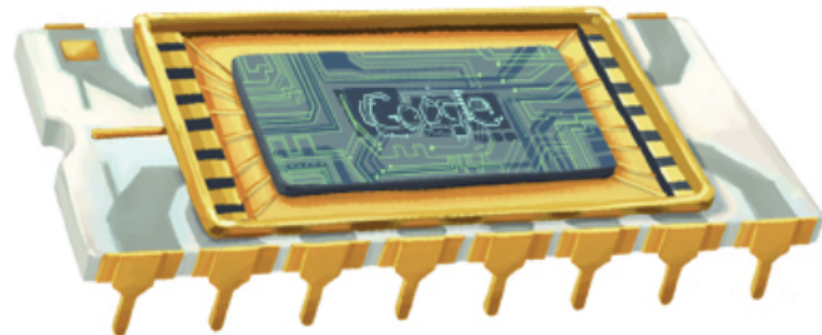
Herbert Kroemer
Prize share: 1/4



Jack S. Kilby
Prize share: 1/2

The Nobel Prize in Physics 2000 was awarded "for basic work on information and communication technology" with one half jointly to Zhores I. Alferov and Herbert Kroemer "for developing semiconductor heterostructures used in high-speed- and opto-electronics" and the other half to Jack S. Kilby "for his part in the invention of the integrated circuit".

Robert Noyce, Fairchild/Intel
Integrated Circuit (1959)



Google Doodle December 12, 2011

Back in the 70s

JANESICK (2001) "SCIENTIFIC CHARGE-COUPLED DEVICES" SPIE PRESS MONOGRAPH VOL. PM#3, P.4.

DATE 19 Oct. 1969
CASE No 39161-17

Charge "Bubble" Devices:

In collaboration with W.S. Boyle, scheme for moving packets of charge (or the absence of charge) along the surface of a semiconductor was devised. This resulted from discussions between W.S. Boyle and G.E. Smith held on Sept. 8, 1969 and the basic scheme was disclosed to F.H. Smith later that day. The principle is demonstrated by the following specific structure.

A negative voltage applied to the electrodes of the above structure causes a depletion region to form under the electrode. The band bending across section A-A when the voltage is first applied is shown below. As a result of generation-recombination centers in the depletion region and at

W.S. Boyle 10/12/69
G.E. Smith 10/14/69

The Nobel Prize in Physics 2009



Photo: U. Montan
Charles Kuen Kao
Prize share: 1/2

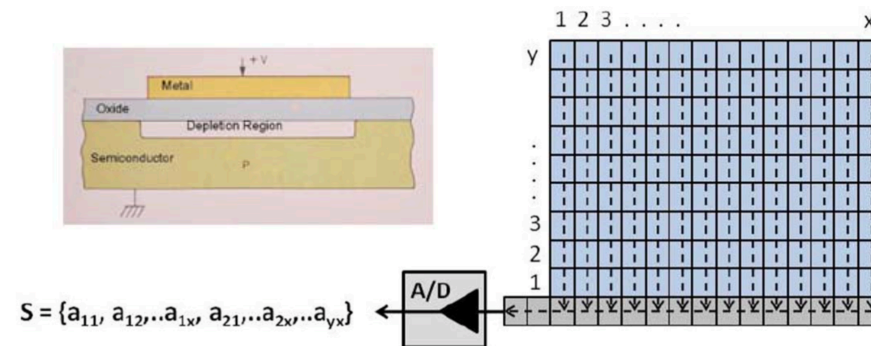


Photo: U. Montan
Willard S. Boyle
Prize share: 1/4



Photo: U. Montan
George E. Smith
Prize share: 1/4

The Nobel Prize in Physics 2009 was divided, one half awarded to Charles Kuen Kao "for groundbreaking achievements concerning the transmission of light in fibers for optical communication", the other half jointly to Willard S. Boyle and George E. Smith "for the invention of an imaging semiconductor circuit - the CCD sensor".



Scientific background on the Nobel prize in Physics 2009

Moore's law

Cramming more components onto integrated circuits

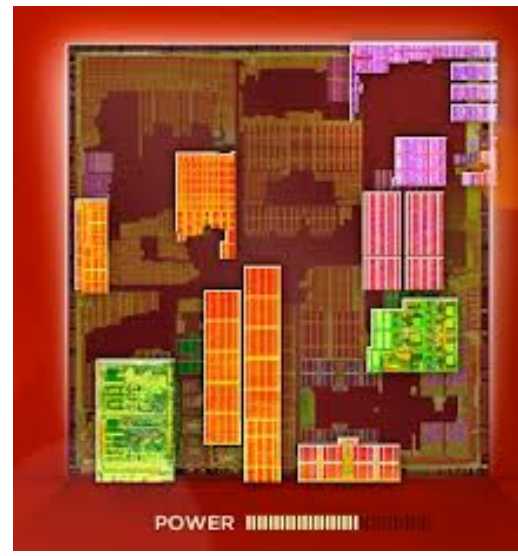
With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

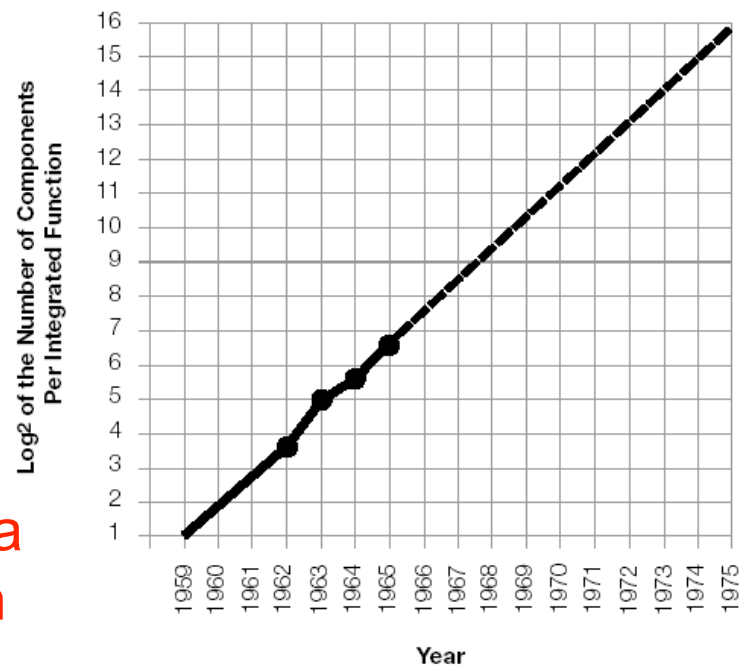
Electronics, Volume 38, Number 8, April 19, 1965



- 1. More transistors per unit silicon area
- 2. Lower energy costs for computation



Snapdragon S4 1 Billion



80s-90s: the heydays of CAD and foundry design

cādence[®]



SYNOPSYS[®]
Predictable Success

Mentor
Graphics[®]

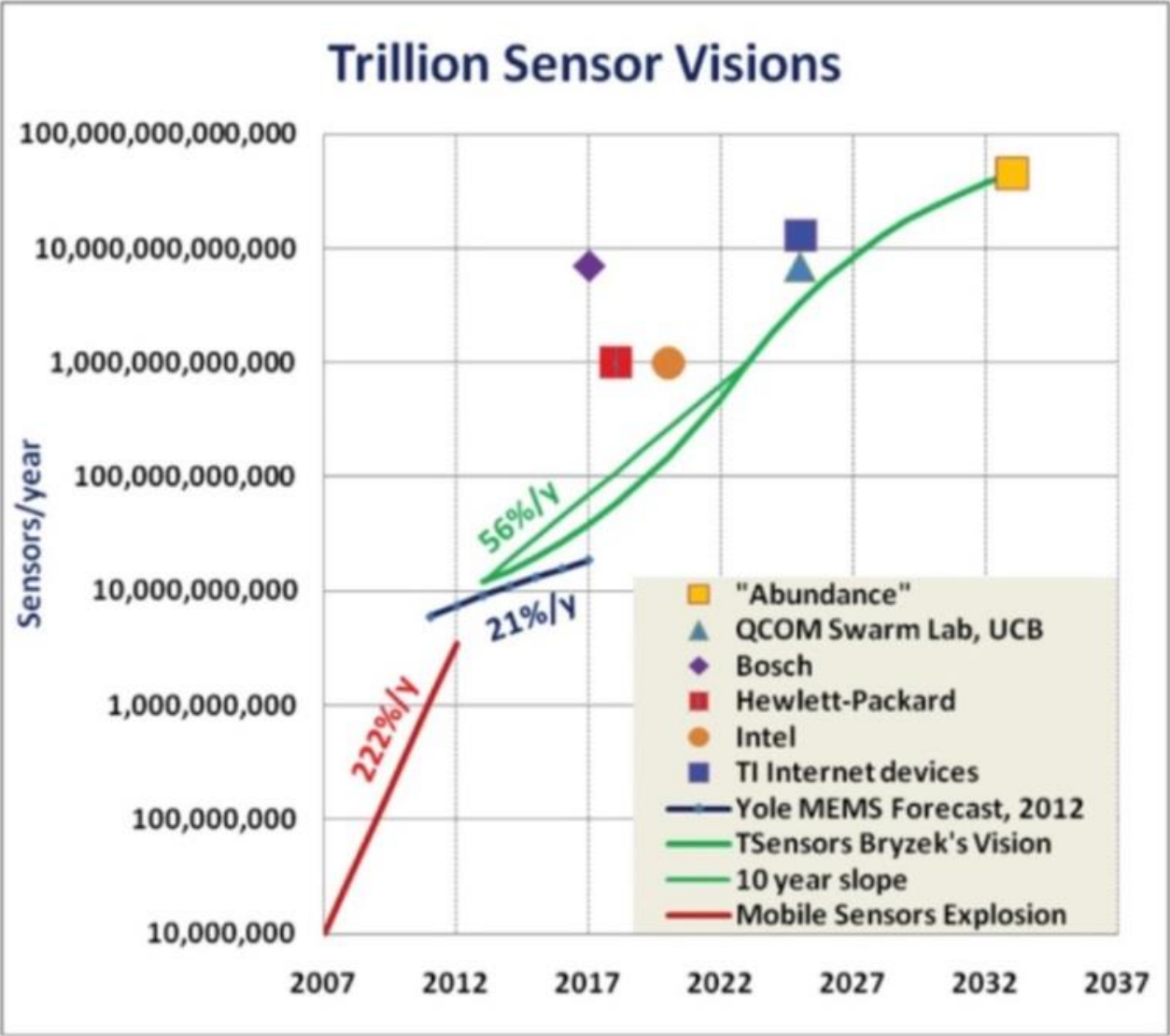
So how do fabricate our own chips?

<http://www.mosis.org/>

Key idea: Use a number of different manufacturers to contribute manufacturing capacity to multiuser projects.

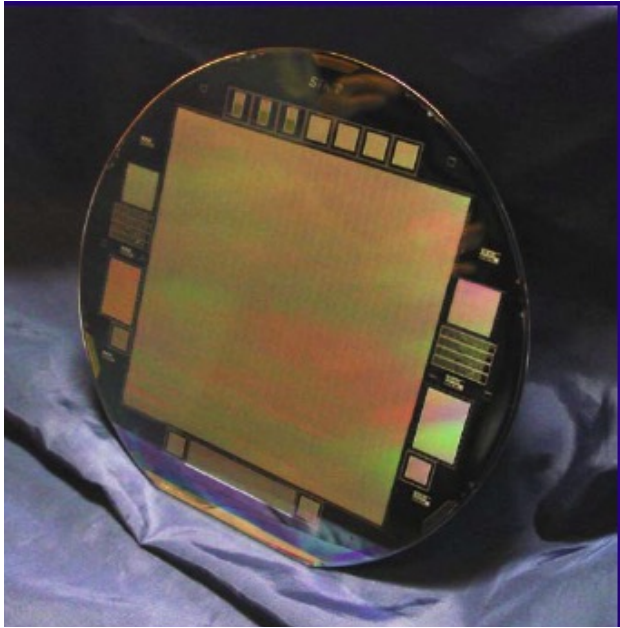
- ON Semiconductor 500 nanometer CMOS
- TSMC 180, 130, 90, 65, 45, 28 nanometer CMOS
- **GF** 180, **130**, 55, 45 nanometer BiCMOS
- IBM 45 nanometer SOI CMOS!

sensors growth



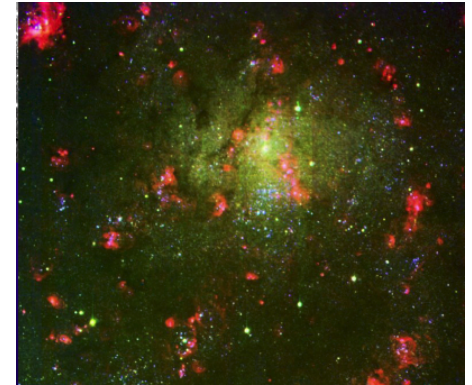
Rebooting the IT Revolution: A Call to Action, SRC, Sept 2015

Late 90s CCD to CMOS: the paradigm shift in camera technologies



CCD state of the art

Full 6 inch wafer
111,000,000 pixels
1 frame per second!



\$10,000,000

Semiconductor Technology Associates

CMOS APS Cameras

1,200,000 / 8,000,000
pixels



\$1 / \$15

20,000,000 pixels



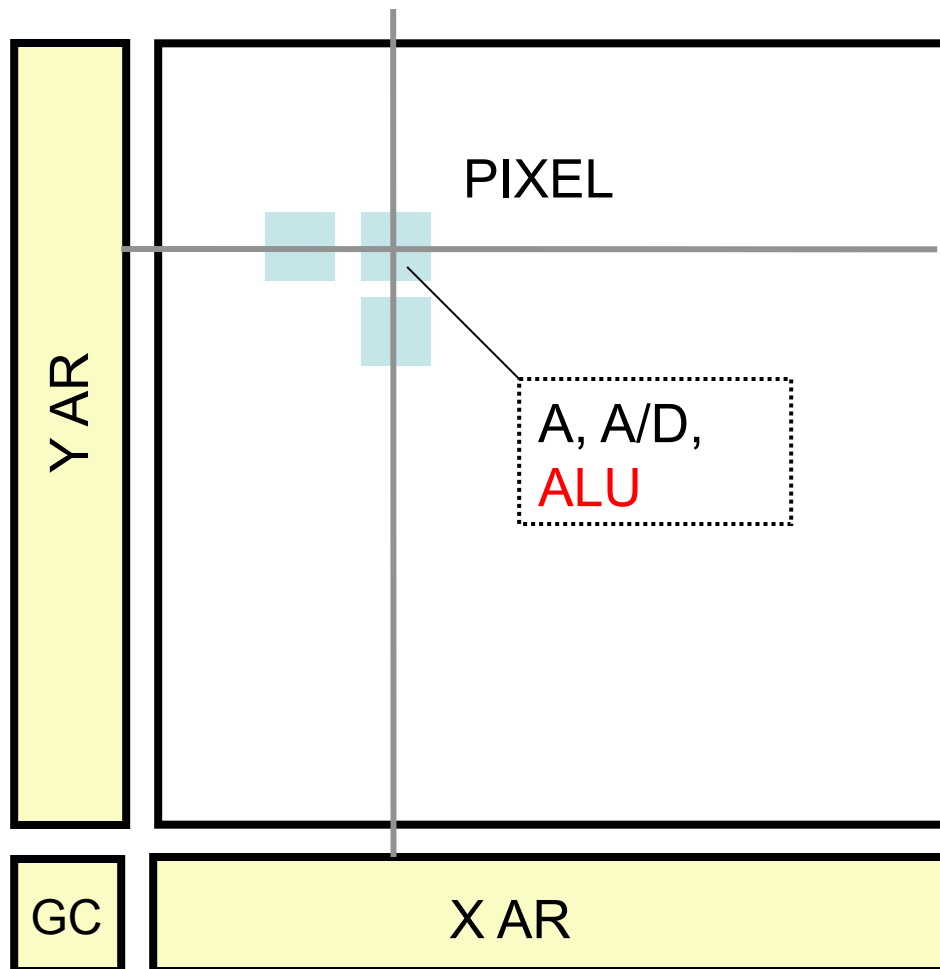
\$200

120,000,000 pixels



\$ 1,000,000

CMOS-APS and digital



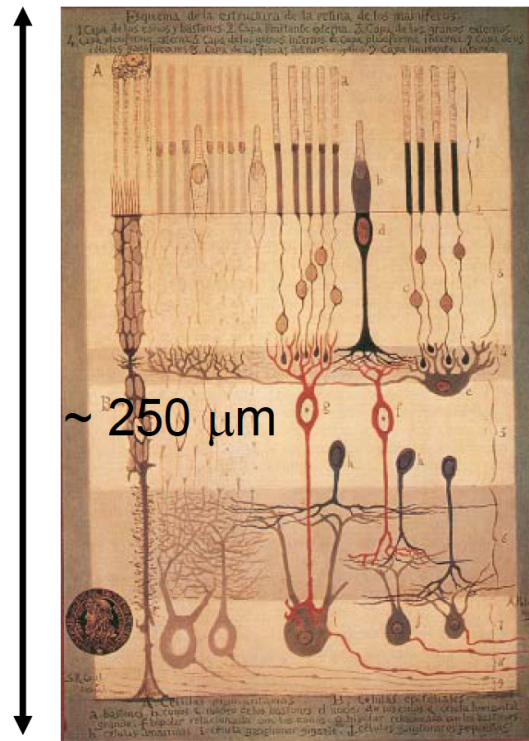
Pixel:

amplification (A)
quantization (A/D)
local asynchronous integration
gain and offset correction

Periphery:

column intensity accumulator (CAC)
global intensity accumulator (GAC)
asynchronous readout (AR)
global control (GC)

combining silicon rods and cones in a single pixel, with event based asynchronous readout



Santiago Ramon y Cajal

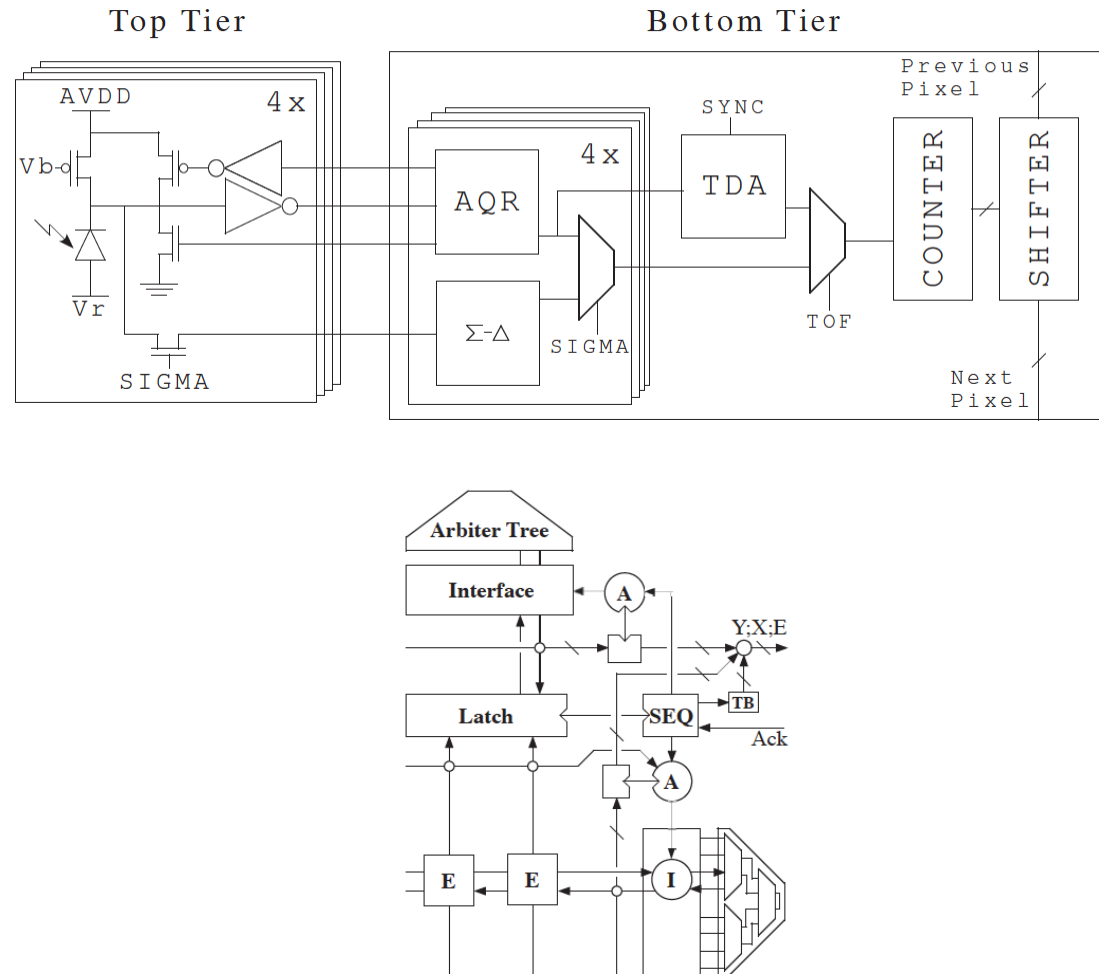
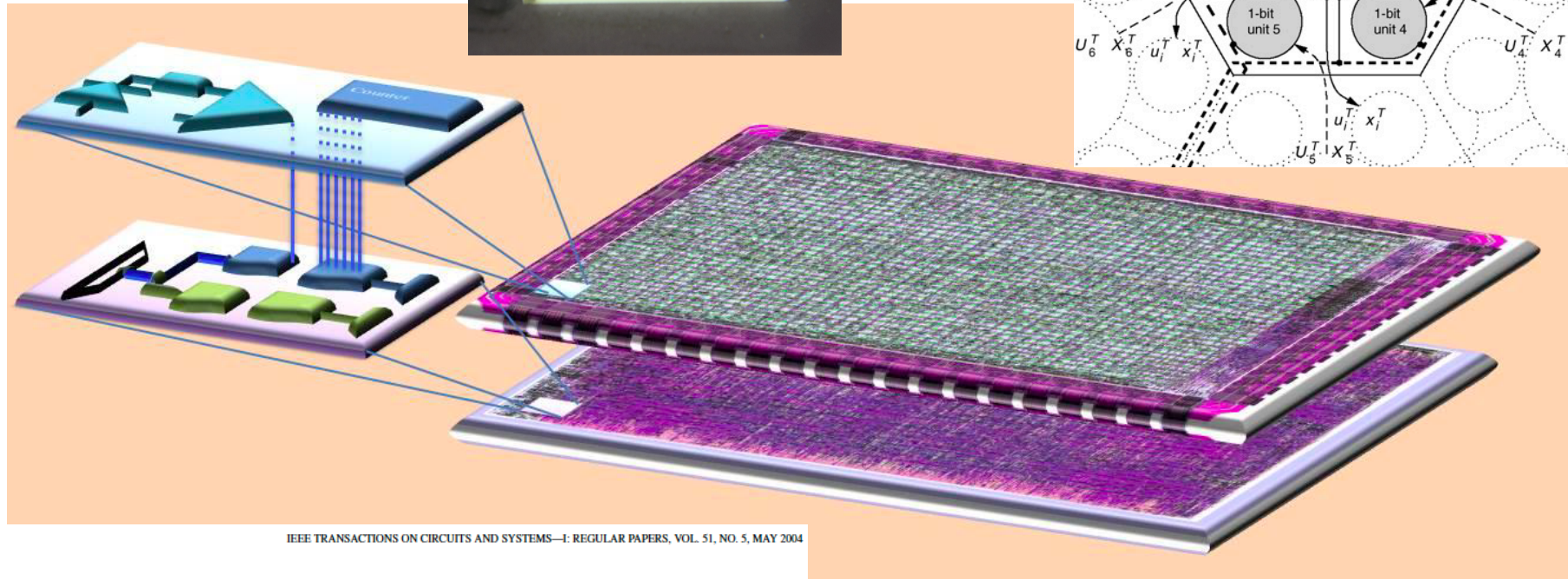
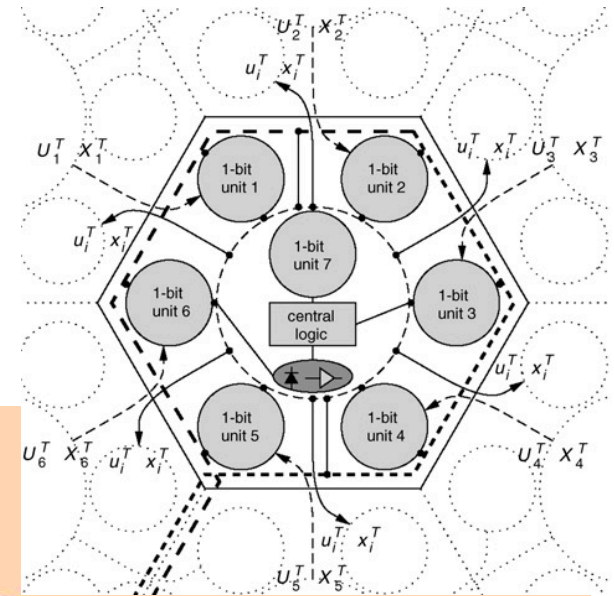
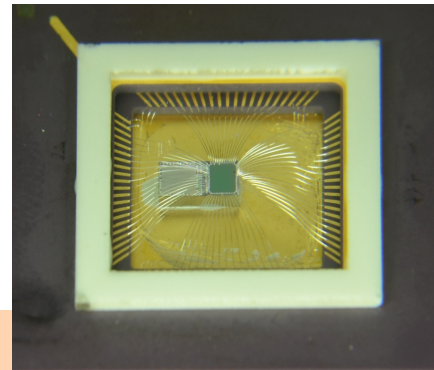


Fig. 5. Asynchronous Readout Architecture The selected row's events are readout in parallel and transmitted in a single packet—row address (Y), column address(es) (X), and tailword (E, generated by TB).

unpublished results from first silicon
(Tezzaron 130nm 3D-CMOS)



Multivariate Function Approximator Chip in 3D CMOS

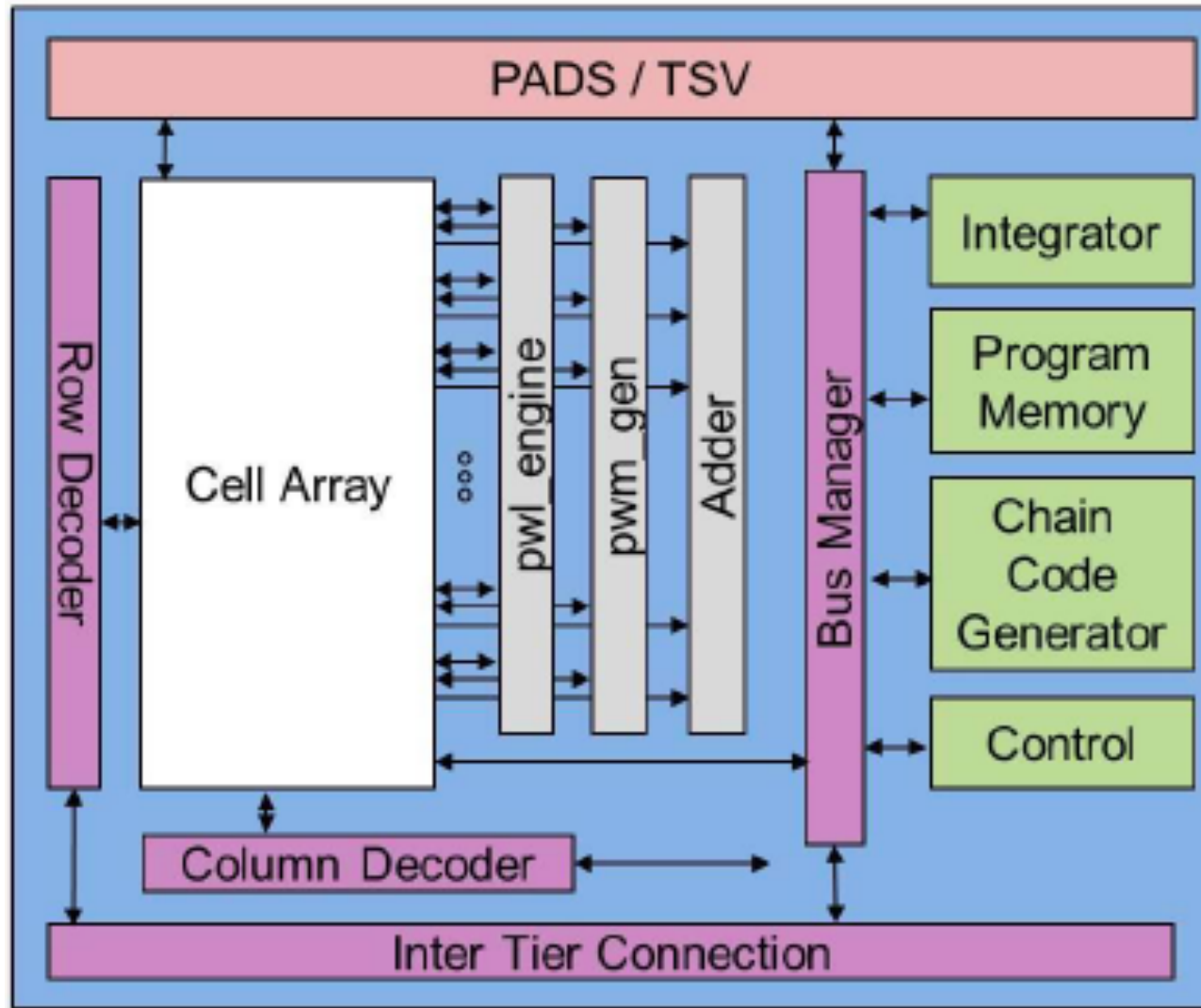


IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 51, NO. 5, MAY 2004

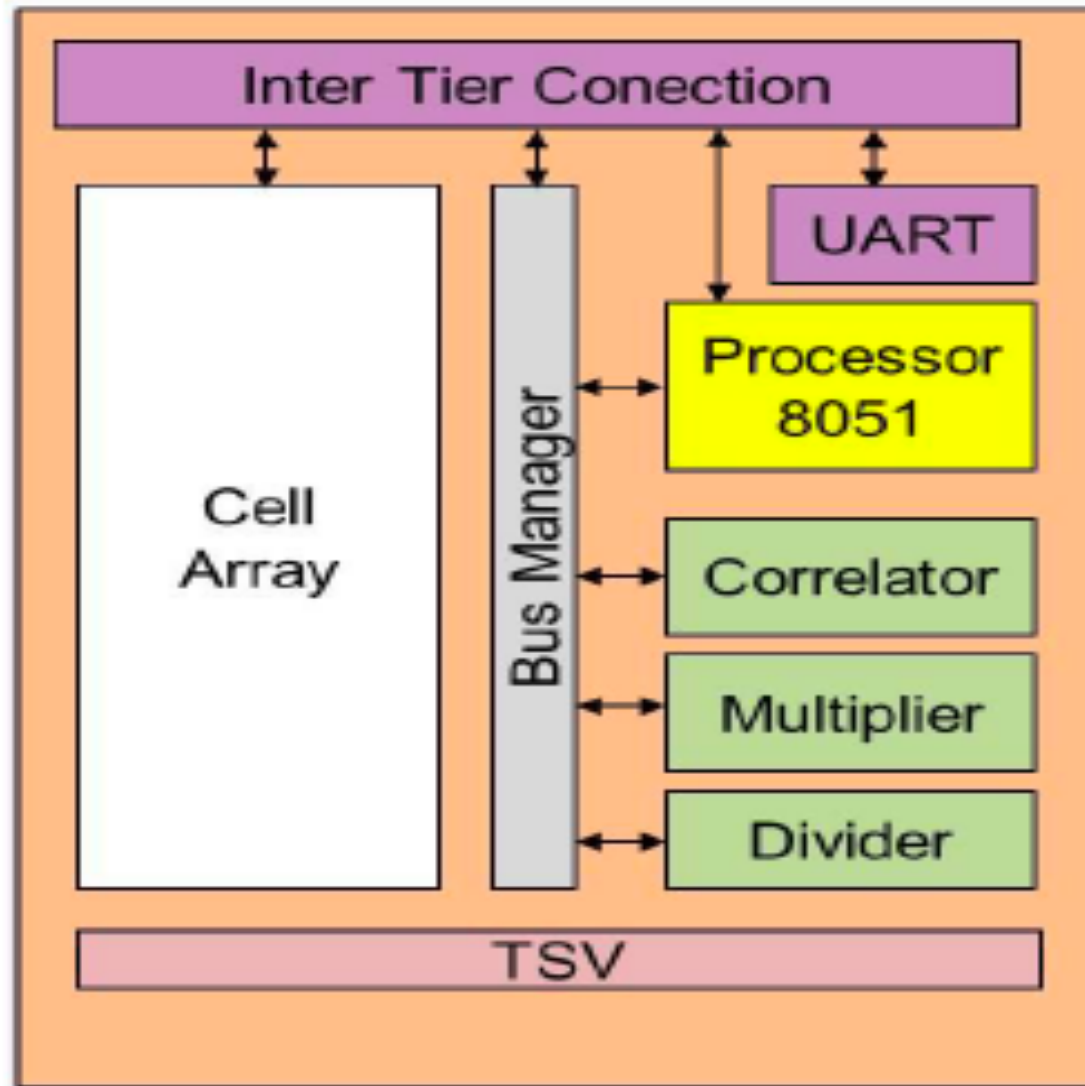
A Scalable and Programmable Simplicial CNN Digital Pixel Processor Architecture

Pablo S. Mandolesi, *Member, IEEE*, Pedro Julián, *Member, IEEE*, and Andreas G. Andreou, *Member, IEEE*

Tezzaron 3D-CMOS Tier 1:



Tezzaron 3D-CMOS Tier 2:



unpublished results from first silicon

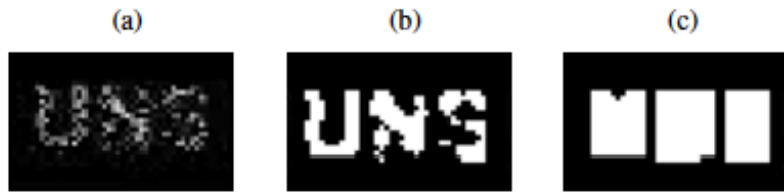


TABLE IV: a) Captured image b) Binarization c) Block recognition

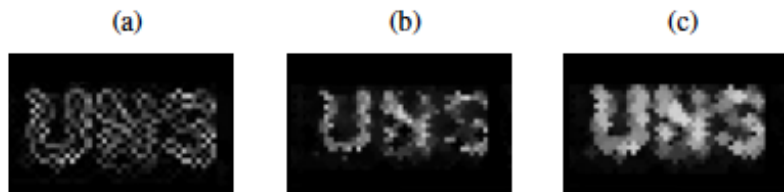


TABLE V: a) Border recognition b) Median Filter c) Dilation

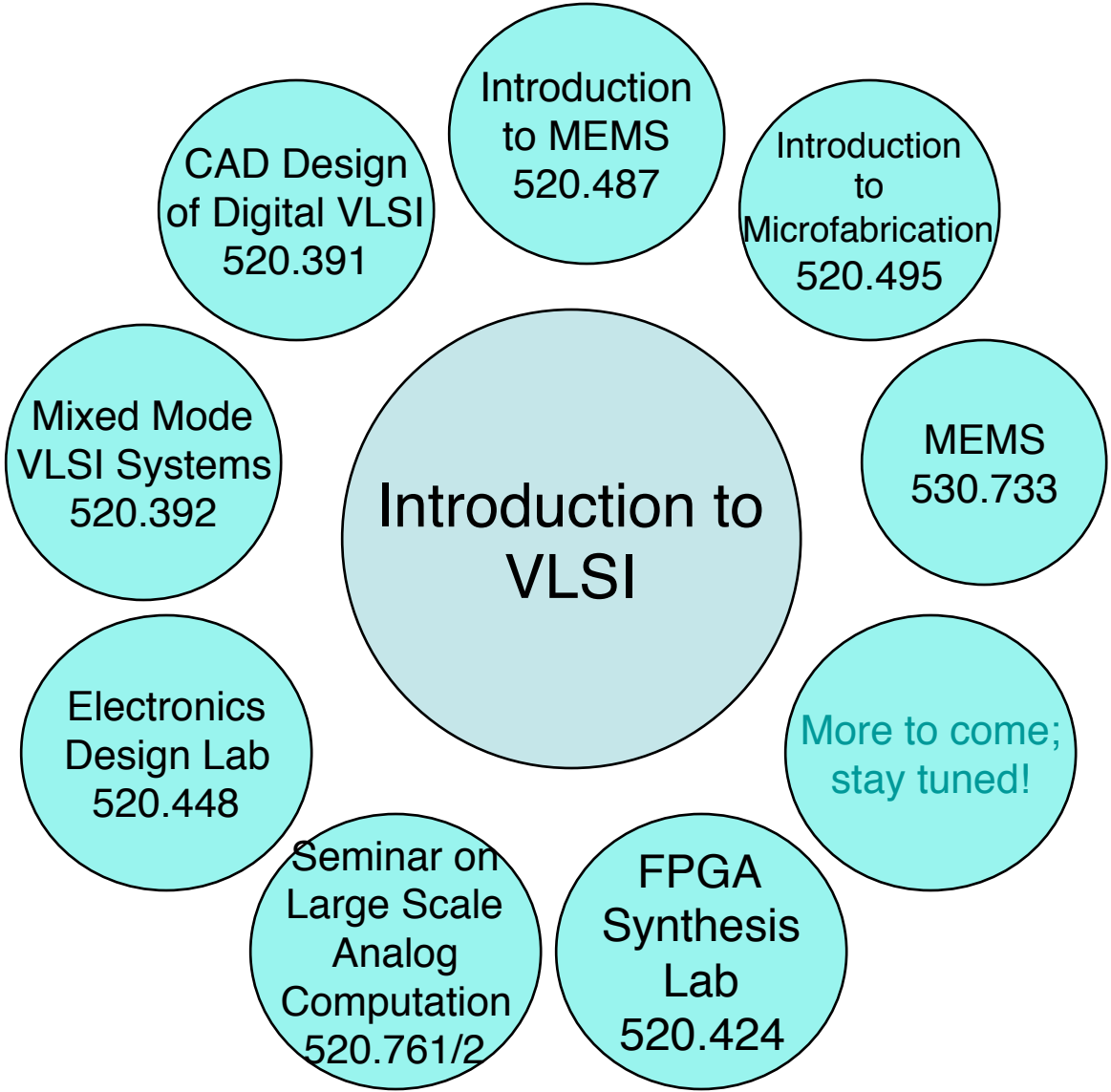
Parameter	Value
Technology	130nm
Die Size	2x2.5mm ²
Cell Size	25x25 μm^2
Resolution	48 x 32
Photodiode Type	n+/p-Substrate
Power Supply	1.5V

Example: Counting objects in an image, by using a bounding box and erosion without figure elimination.

```

%Capture Image
:BOUNDING
LOAD FUNCTION_F(Bounding)
LOAD FUNCTION_G(Zeros)
Conf = "00000001" ;Border="0", Nei=+, FoG=OR
CNNProcess(CNN, Conf)
WAIT until CNNProcess end
LOAD Counter_on_U
IF image_X = image_U
goto REDUCE
else
LOAD Counter_on_X
goto BOUNDING
end
:REDUCE
repeat 24
LOAD FUNCTION_F(Point_Reduction)
LOAD FUNCTION_G(Zeros)
Conf = "00000001" ;Border="0", Nei=+, FoG=OR
CNNProcess(CNN, Conf)
WAIT until CNNProcess end
LOAD Counter_on_X
end
%Count all the pixels
RST Integrator
for ind=0:47
COL = ind
INTEGRATE
end
SELBUSOUT (INTEGER)
    
```

520.216 and her friends



Life after Intro VLSI course (I)



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Silicon Labs Management

Tyson Tuttle

Chief Executive Officer



Mr. Tuttle joined Silicon Labs in 1997 and helped design the company's first product, a silicon DAA, that subsequently achieved market share leadership in PC modems and allowed the company to go public in 2000. Mr. Tuttle led the marketing effort behind the company's first RF transceiver products for mobile handsets. He also spearheaded the development and market penetration strategy of the company's successful radio and TV tuner ICs, creating the broadcast business that today represents about one third of the company. Mr. Tuttle led the broadcast product lines until 2010 when the R&D team was consolidated under his leadership as chief technology officer. He then took over as chief operating officer in 2011 and was responsible for managing all of the company's business units and R&D. He became the CEO in 2012. Prior to joining Silicon Labs, Mr. Tuttle held senior design engineering positions at Crystal Semiconductor/Cirrus Logic and Broadcom Corporation. Mr. Tuttle holds an M.S. in electrical engineering from UCLA and a B.S. in electrical engineering from Johns Hopkins University. He has 70 patents issued or pending in the areas of RF and mixed-signal IC design.

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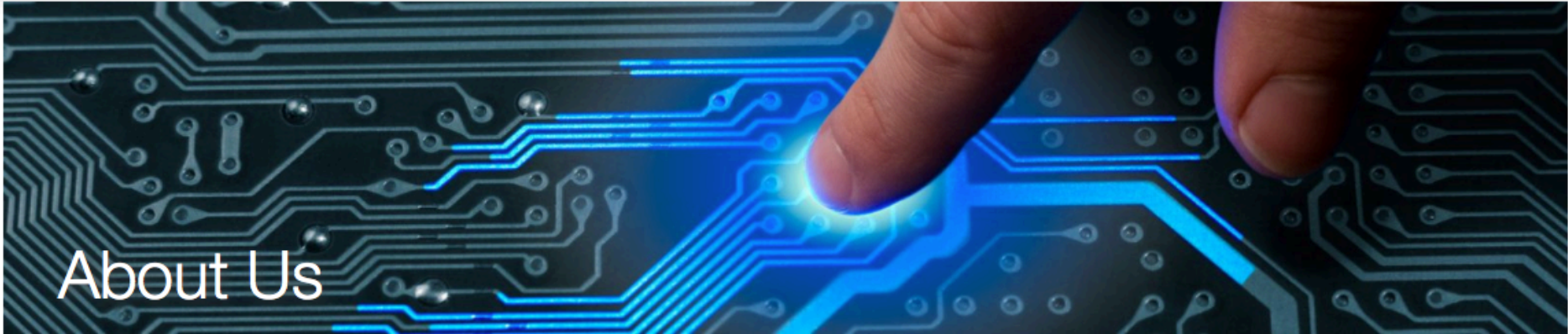


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Jumpstart your next Internet of Things design with our new SENSOR-PUCK development and demo platform. Featuring our Si114x Optical Sensors and Si701x/2x Relative Humidity and Temperature Sensors, the board is controlled by an EFM32 energy friendly MCU giving you easy measurement of finger tip heart rate, UV index, ambient light, relative humidity and temperature.

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Life after 520.216 (II)



Kewei Yang Chairman and CEO

Throughout his career, Kewei Yang has focused on high-speed analog and mixed-signal design. Before co-founding Analogix, he was vice-president of engineering at Mindspeed, a division of Conexant, where he directed the company's development of high-speed transceivers and switch fabric ICs. He came to Conexant via its acquisition of HotRail, where he served as chief scientist. He also served as a lead designer at Rendition, a graphics chip company, and at Hewlett-Packard in the Computer Technology Lab.

Yang has a B.S. degree in electrical engineering from Tsinghua University and an M.S. degree in electrical engineering and Ph.D. from Johns Hopkins University.



Life after intro VLSI (III)



This could be you!

CEO of Johns Hopkins on the Chip

Johns Hopkins on the chip: microsystems and cognitive machines for sustainable, affordable, personalised medicine and healthcare

A.G. Andreou

Semiconductor technology is contributing to the advancement of biotechnology, medicine and healthcare delivery in ways that it was never envisioned – from chip micro-arrays, to scientific grade CMOS imagers and ion sensing arrays to implantable prosthesis. This exponential growth of sensory microsystems has led to an exponential growth of data. Cognitive machines, i.e. advanced computer architectures and algorithms, are carefully co-designed to extract knowledge from such health data making rational decisions and recommendations for therapies. Nano, micro and macro robotics driven by sophisticated algorithms interface to the human body at different levels and scales, from nano-scale molecules to micron-scale cells to networks and all the way to the scale of organisms. The present era is one where semiconductor technology and the ‘chip’ is the foundation of sustainable and affordable personalised medicine and healthcare delivery.

Class Objectives

520.216 will teach you you how to go from a simple idea to a system, a CMOS camera chip. You will do analysis, design and finally layout and simulation and fabricate your own chip!

Emphasis is in physical design principles.

Computer Aided Design Tools

