Chapter 11

Transistor characteristics

11.1 Basic transistor characteristics

Given an individual NFET (or PFET), we can apply known voltages to its terminals and measure the current flowing in to (or out of) the drain terminal. For instance, given the definition of terminal voltages and positive drain current[1] as shown in Figure 11.1, we get the characteristics shown in Figures 11.2 and 11.3, when the source and bulk terminals are fixed at zero. Note that the drain and gate terminal voltages are negative in this instance because the source and bulk terminals are taken to be at zero volts instead of Vdd.

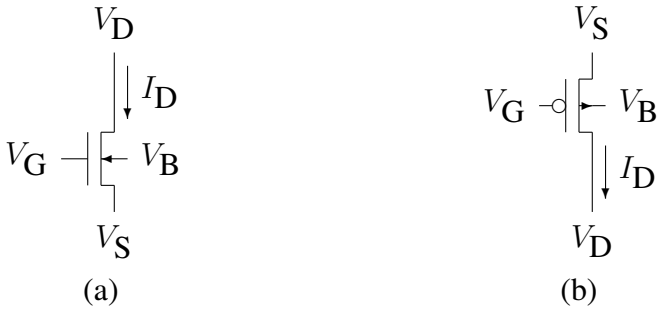

Figure 11.1: Definition of terminal voltages and positive drain current. (a) NFET. (b) PFET.

The first principal features of these curves is that for a given gate voltage, as the drain voltage increase in magnitude from zero, the drain current initially increases proportionately. Then, at some point, the drain current saturates, that is it becomes more or less constant, increasing only slightly with further increases in the magnitude of the drain voltage. These two regions are named the *triode* (or *linear* or *ohmic*) region and the *saturation* (or *active*) region respectively.

The second principal features of these curves is that the spacing between the saturation currents increases with the magnitude of the gate voltage. That is, the difference between the saturation current for $|V_G| = 5$V and $|V_G| = 4$V is larger than the difference between the saturation current for $|V_G| = 3$V and $|V_G| = 2$V.

[1]Not that the given definition of positive drain current for the PFET is opposite of the convention used in many textbooks.

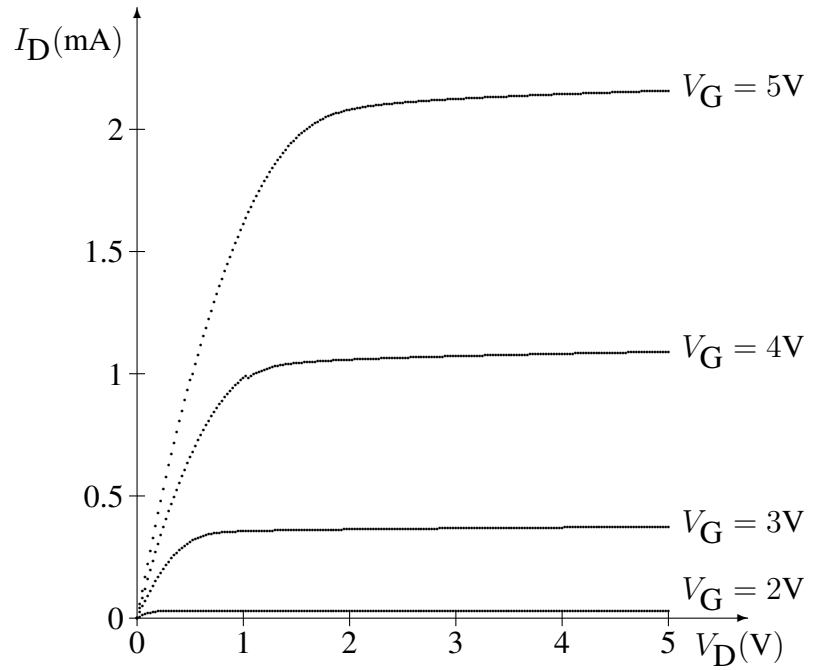

Figure 11.2: NFET drain current (I_{D}) versus drain voltage (V_{D}) with $V_{\mathrm{S}} = 0$V and $V_{\mathrm{B}} = 0$V.

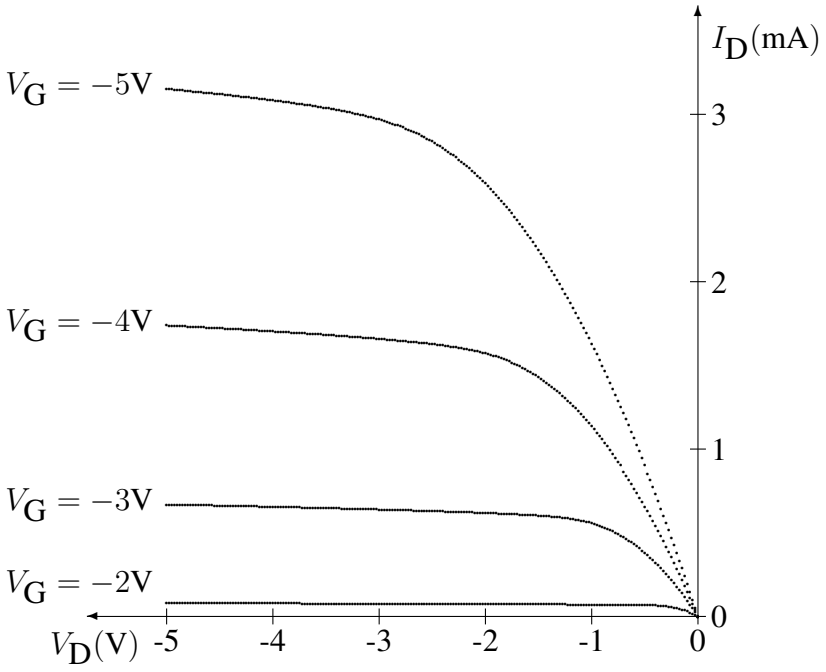

Figure 11.3: PFET drain current (I_{D}) versus drain voltage (V_{D}) with $V_{\mathrm{S}} = 0$V and $V_{\mathrm{B}} = 0$V.

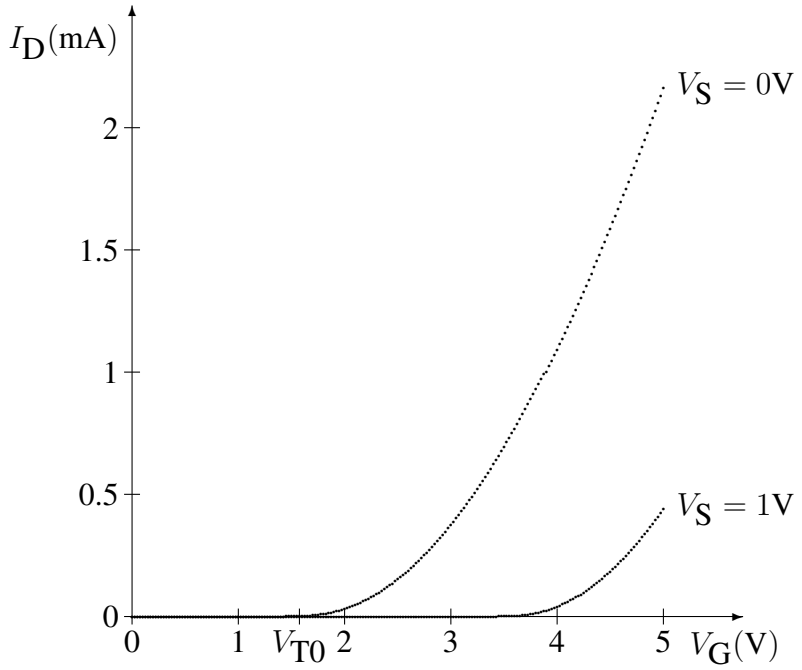

Figure 11.4: NFET drain current (I_{D}) versus gate voltage (V_{G}) with $V_{\mathrm{D}} = 5$V and $V_{\mathrm{B}} = 0$V with $V_{\mathrm{S}} = 0$V and $V_{\mathrm{B}} = 0$V.

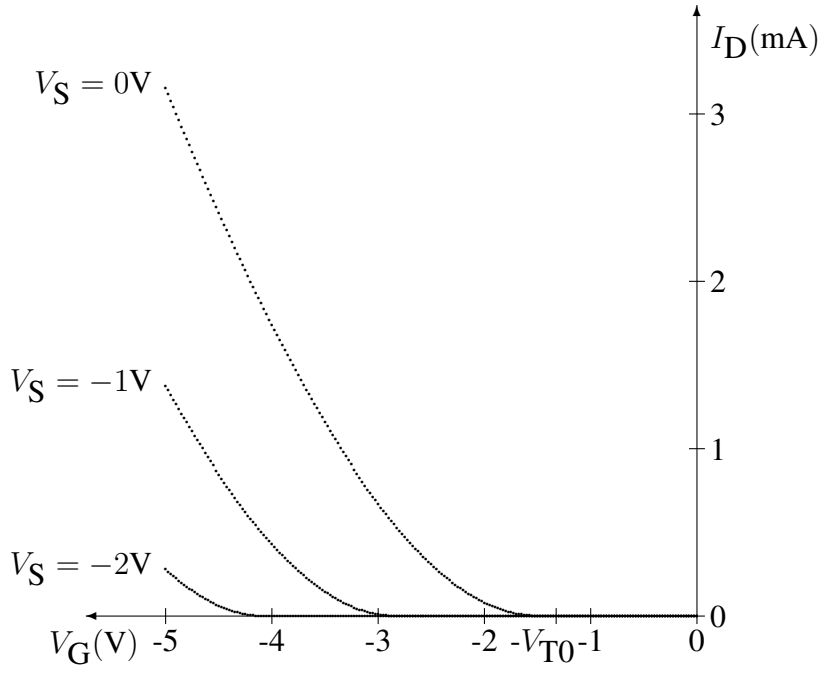

Figure 11.5: PFET drain current (I_{D}) versus gate voltage (V_{G}) with $V_{\mathrm{D}} = -5$V and $V_{\mathrm{B}} = 0$V.

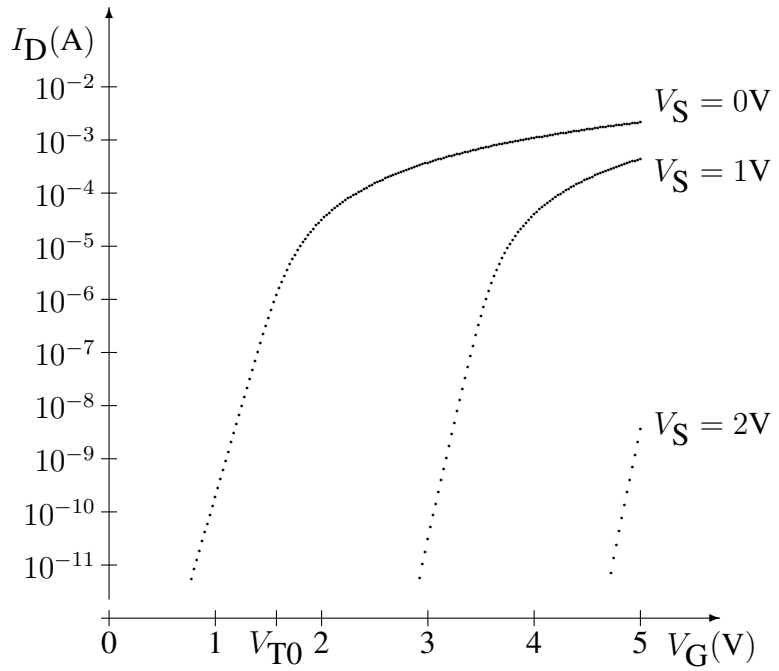

Figure 11.6: NFET drain current (I_{D}) versus gate voltage (V_{G}) with $V_{\mathrm{D}} = 5$V and $V_{\mathrm{B}} = 0$V.

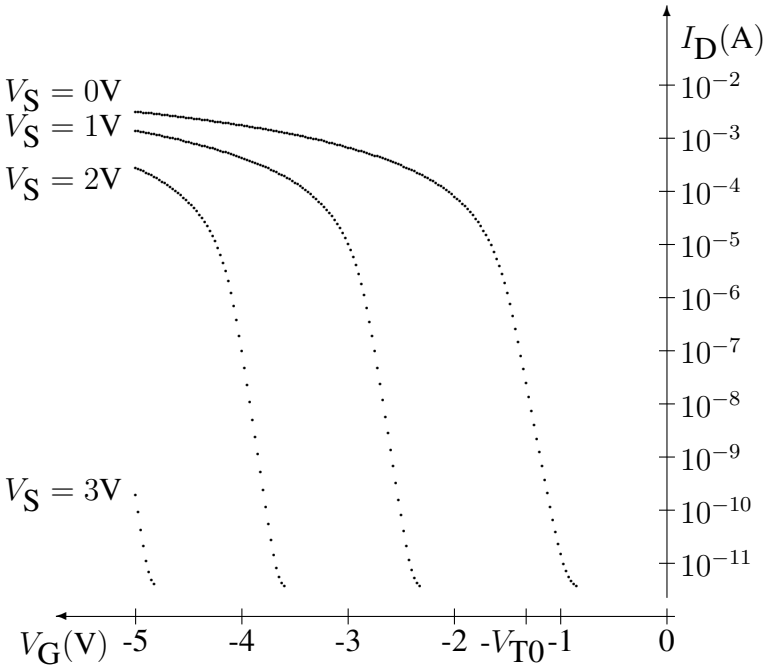

Figure 11.7: PFET drain current (I_{D}) versus gate voltage (V_{G}) with $V_{\mathrm{D}} = -5$V and $V_{\mathrm{B}} = 0$V.

We can investigate the effect of the gate voltage on the drain current by fixing the drain voltage and plotting the drain current versus the gate voltage. This give us the characteristics shown in Figures 11.4 and 11.5. These show that the drain current approximately follows a square-law with respect to the gate voltage, provided that the gate voltage is above a minimum threshold V_{T0}. These curves also show that the threshold increases when the magnitude of the source voltage increases.

For the NFET, these characteristics can be modeled with the following set of simple equations:

$$I_{\mathrm{D}} = \frac{k_n'}{2}\frac{W}{L}\left[(V_{\mathrm{G}} - V_{\mathrm{S}}) - V_{\mathrm{T}}\right]^2\left[1 + \lambda(V_{\mathrm{D}} - V_{\mathrm{S}})\right] \quad \text{for} \quad (V_{\mathrm{D}} - V_{\mathrm{S}}) \geq (V_{\mathrm{G}} - V_{\mathrm{S}}) - V_{\mathrm{T}}$$

and

$$I_{\mathrm{D}} = k_n'\frac{W}{L}\left\{\left[(V_{\mathrm{G}} - V_{\mathrm{S}}) - V_{\mathrm{T}}\right](V_{\mathrm{D}} - V_{\mathrm{S}}) - \frac{(V_{\mathrm{D}} - V_{\mathrm{S}})^2}{2}\right\} \quad \text{for} \quad (V_{\mathrm{D}} - V_{\mathrm{S}}) < (V_{\mathrm{G}} - V_{\mathrm{S}}) - V_{\mathrm{T}}$$

with

$$V_{\mathrm{T}} = V_{\mathrm{T0}} + \gamma\left[\sqrt{-2\phi_{\mathrm{F}} - (V_{\mathrm{B}} - V_{\mathrm{S}})} - \sqrt{-2\phi_{\mathrm{F}}}\right]$$

These equations are valid for $V_{\mathrm{G}} - V_{\mathrm{S}} > V_{\mathrm{T}}$, and assume that $I_{\mathrm{D}} = 0$ otherwise. However, by plotting the data for Figures 11.4 and 11.5 on a semilog scale (Figures 11.6 and 11.7), it is clear that the current doesn't go to to zero immediately at the threshold, but rather decreases exponentially.

In this subthreshold region of operation, the NFET characteristics can be modeled with the following equation:

$$I_{\mathrm{D}} = I_0 e^{\frac{\kappa(V_{\mathrm{G}} - V_{\mathrm{B}})}{V_t}}\left(e^{\frac{V_{\mathrm{B}} - V_{\mathrm{S}}}{V_t}} - e^{\frac{V_{\mathrm{B}} - V_{\mathrm{D}}}{V_t}}\right)$$

where V_t is the thermal voltage, not the threshold voltage.

The equations for the PFET can be obtained by replacing V_{G}, V_{S}, V_{D} and V_{B} with $-V_{\mathrm{G}}$, $-V_{\mathrm{S}}$, $-V_{\mathrm{D}}$ and $-V_{\mathrm{B}}$ in the equations for the NFET.

11.2 Basic inverter characteristics

If we connect an NFET and a PFET together to form an inverter as shown in Figure 11.8, we can plot the characteristics of this logic gate.

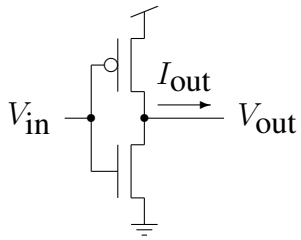

Figure 11.8: Definition of input and output voltages and positive output current.

If nothing is connected to the output of the inverter ($I_{\mathrm{out}} = 0$), then we get the characteristics shown in Figure 11.9. In this instance, when the input is less than 2.65 V, the drain current from

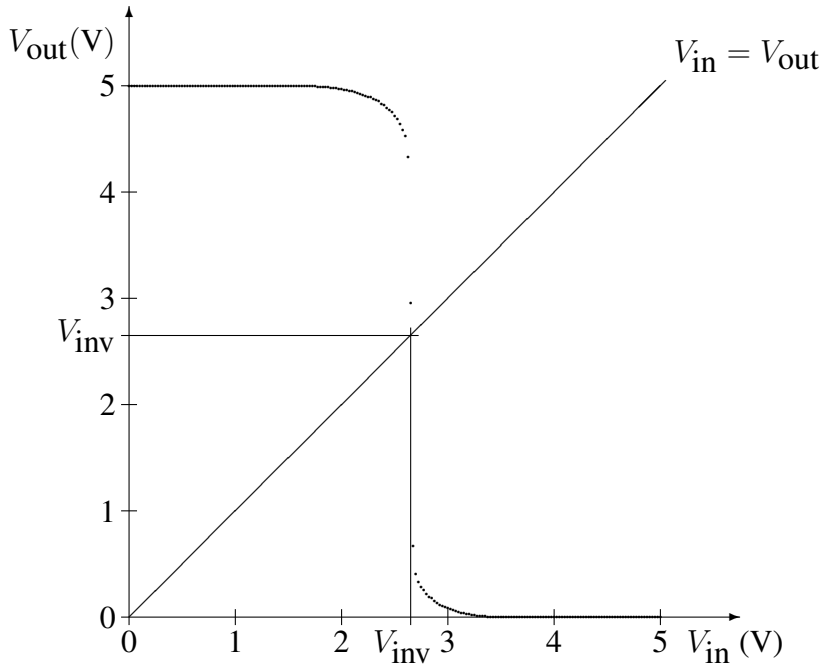

Figure 11.9: Inverter output voltage (V_{out}) versus input voltage (V_{in}).

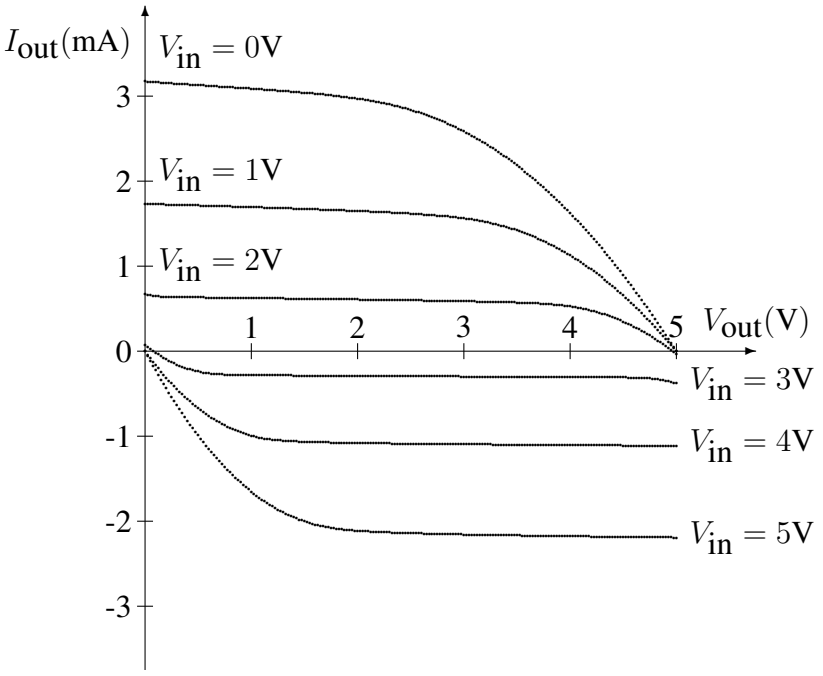

Figure 11.10: Inverter output current (I_{out}) versus output voltage (V_{out}).

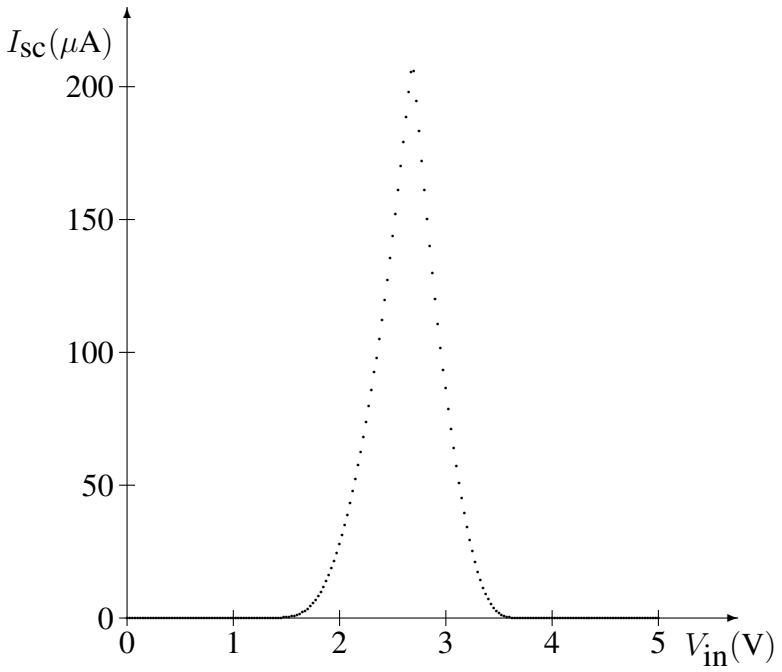

Figure 11.11: Inverter short-circuit current (I_{sc}) versus input voltage (V_{in}).

the PFET exceeds the drain current from the NFET and the output is high. Alternately, when the input is greater than 2.65 V, the drain current from the NFET exceeds the drain current from the PFET and the output is low.

Under normal circumstances, the output of a logic gate is connected to the input of another logic gate, and I_{out} is used to charge or discharge the input capacitance of the latter. The current available for charging and discharging is shown in Figure 11.10. When $V_{in} = 0$V or 1V, the output current is just the drain current of the PFET as in Figure 11.3 because the drain current of the NFET is negligible. Similarly, when $V_{in} = 5$V or 4V, the output current is just the drain current of the NFET as in Figure 11.2 because the drain current of the PFET is negligible.

However, at more intermediate input voltages, the output current is the difference between the drain current of the PFET and the drain current of the NFET, and a significant portion of the current in the two transistors flows uselessly from Vdd to Gnd. This wasted current is call the *short-circuit current* and can be measured by monitoring the power supply current when $I_{out} = 0$. These characteristics are shown in Figure 11.11.

11.3 Transistor threshold adjustment

The short circuit current and the subthreshold characteristics of transistors are important for integrated circuit manufacturers because they set practical limits on how low the threshold voltage can be set. For a given operating point, lowering the threshold voltage of the transistor supplying the inverter's output current increases the current at the drain terminal of the transistor, and hence the inverter's output current. And increasing the output current of a logic gate increases the speed of the circuit that the logic gate is a part of.

Figure 11.12 shows the drain current of a hypothetical device for four different threshold voltages. As the threshold voltage decreases, the drain current at a given gate terminal voltage (*e.g.* 1 V) increases.

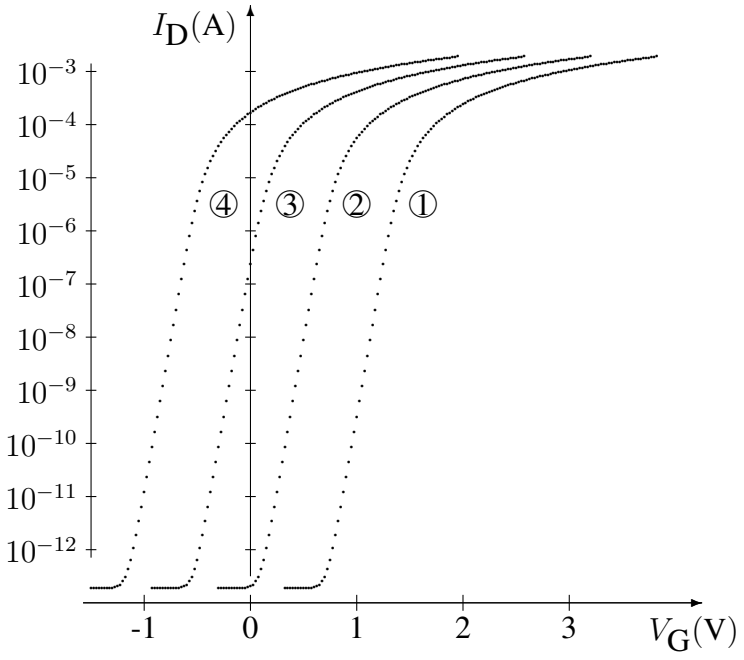

Figure 11.12: Drain current of a hypothetical device for different threshold voltages.

However, as the threshold voltage decreases, the peak short-circuit current will also increase. In fact, if the threshold is too small, then the transistor drain current is no longer negligible even when $V_G = 0$V, so that we get a significant short-circuit current when the input voltage to the inverter is 0 or 5 V (*e.g.* curves 3 and 4).

Another problem with very low thresholds is that difference between the on drain current ($V_G = 5$V) and the off drain current ($V_G = 0$V) can become too small to guarantee switching of the logic gate output. This can happen in a NOR gate for instance where the sum of the NFET off currents may exceed the on current of the series connected PFETs, so that the output never goes high.

Maximizing the ratio of the on current to the off current requires using a high threshold voltage. However, because the drain to bulk junction of the transistor has a small leakage current associated with it, increasing the threshold to where the off current is no longer exponential leads to a reduction in the on to off ratio. Hence curve 2 has the optimum ratio.