520.216

Lecture 5
MOS Transistor Model

Andreas G. Andreou

MOS transistor revisited (I)

Fig. fm1a:

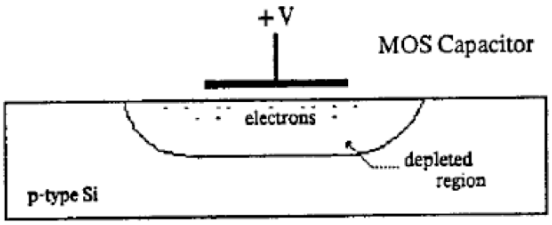


Fig. fm1b:

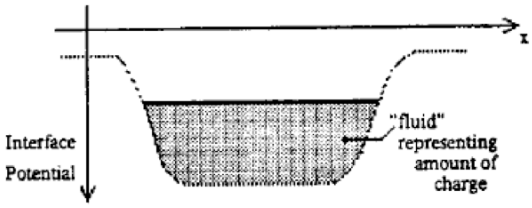


Fig. fm2a:

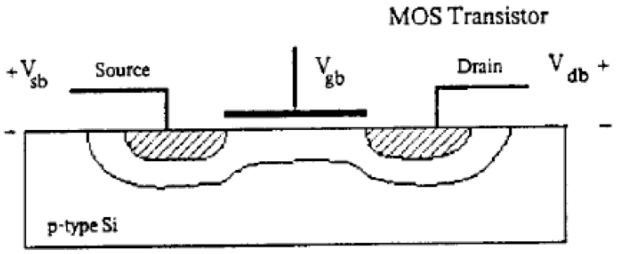
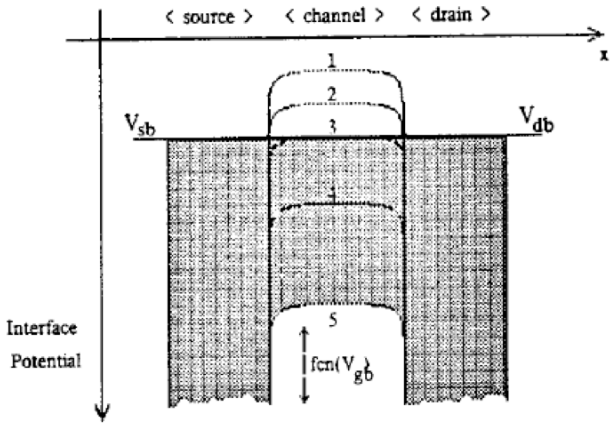
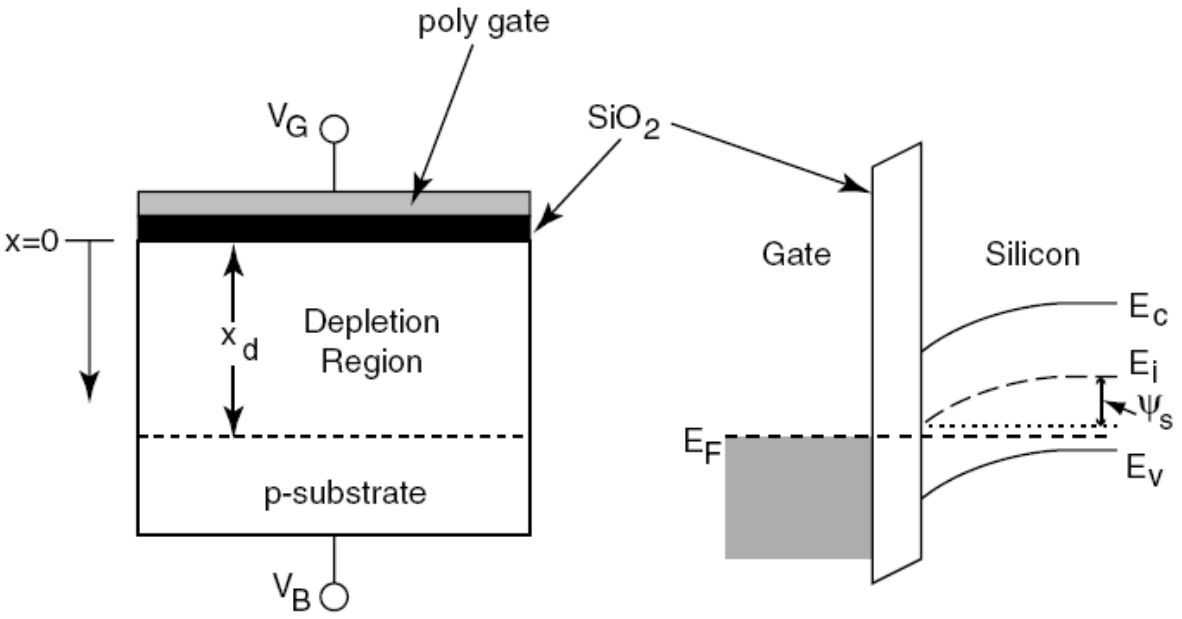


Fig. fm2b:



From: Introduction to VLSI Mead and Conway

MOS structure



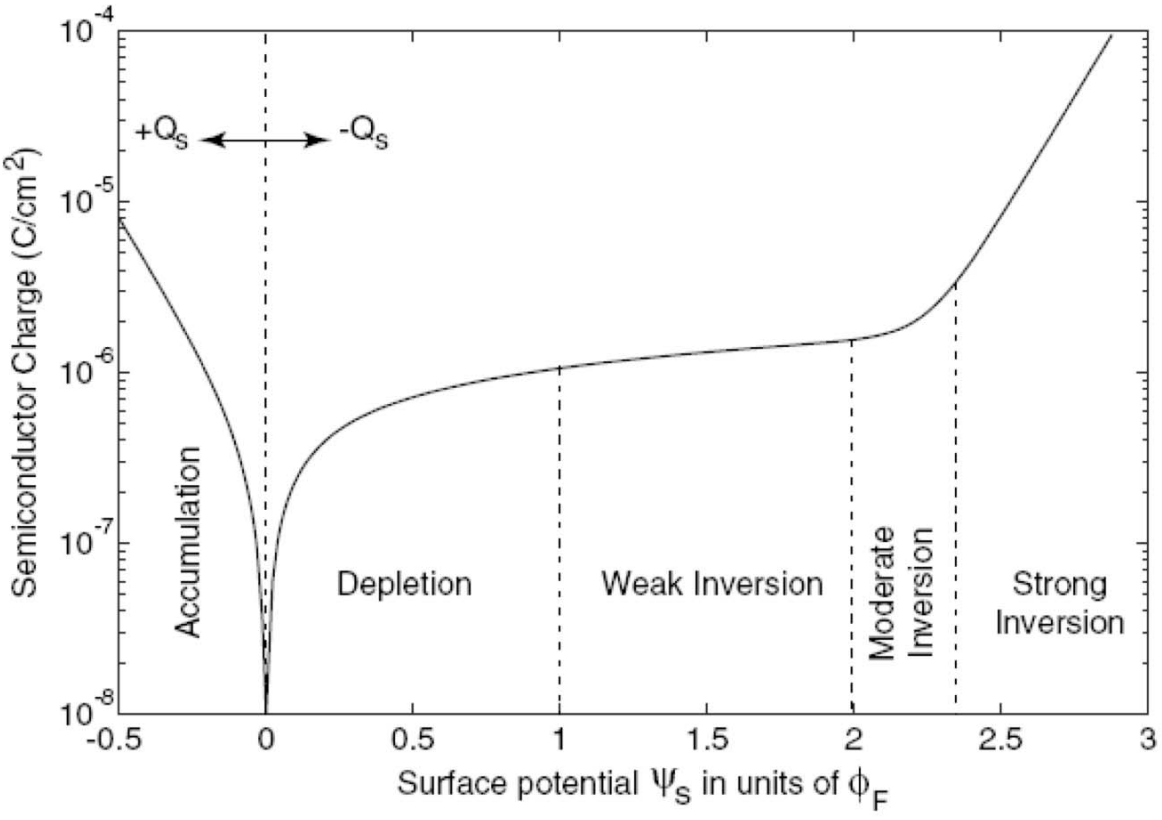
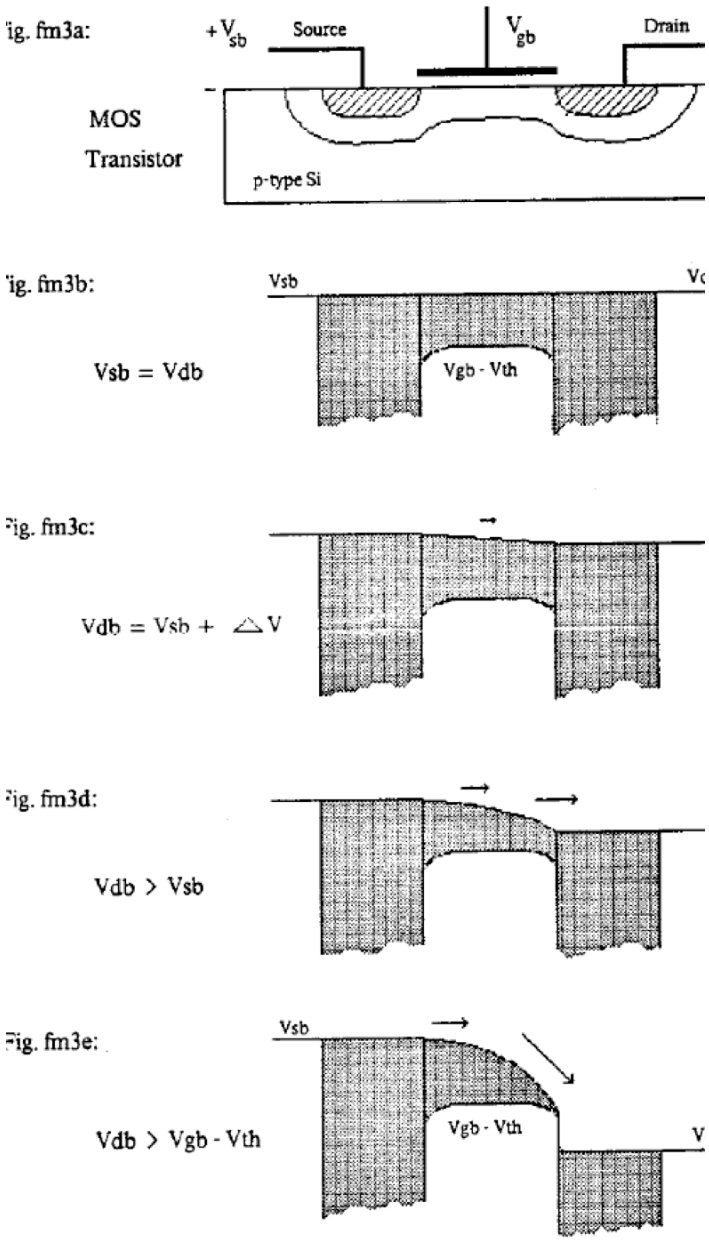


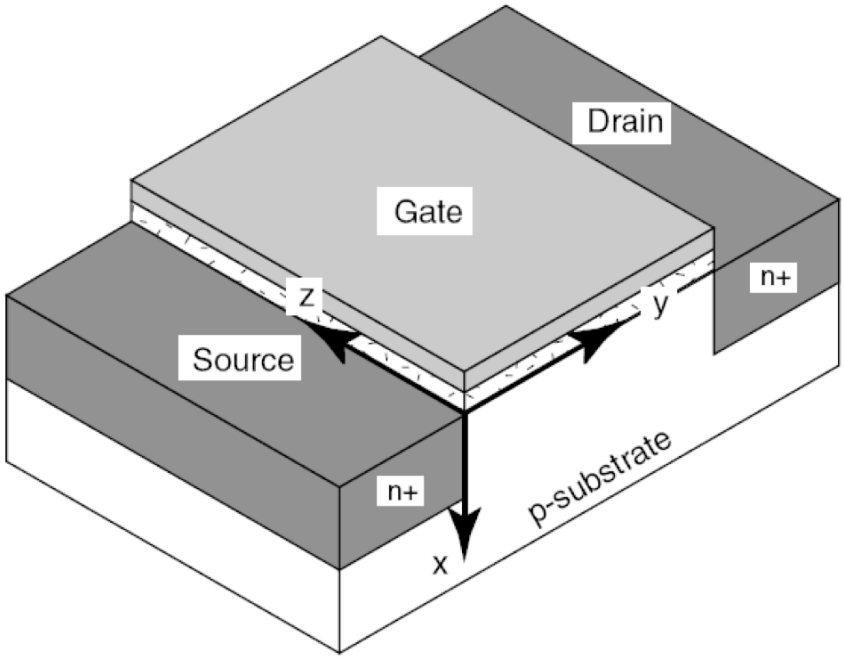
Figure 2.2: Semiconductor charge per cm^2 vs. surface potential for a MOS structure doped at $N_A = 7 \times 10^{15}/\text{cm}^3$.

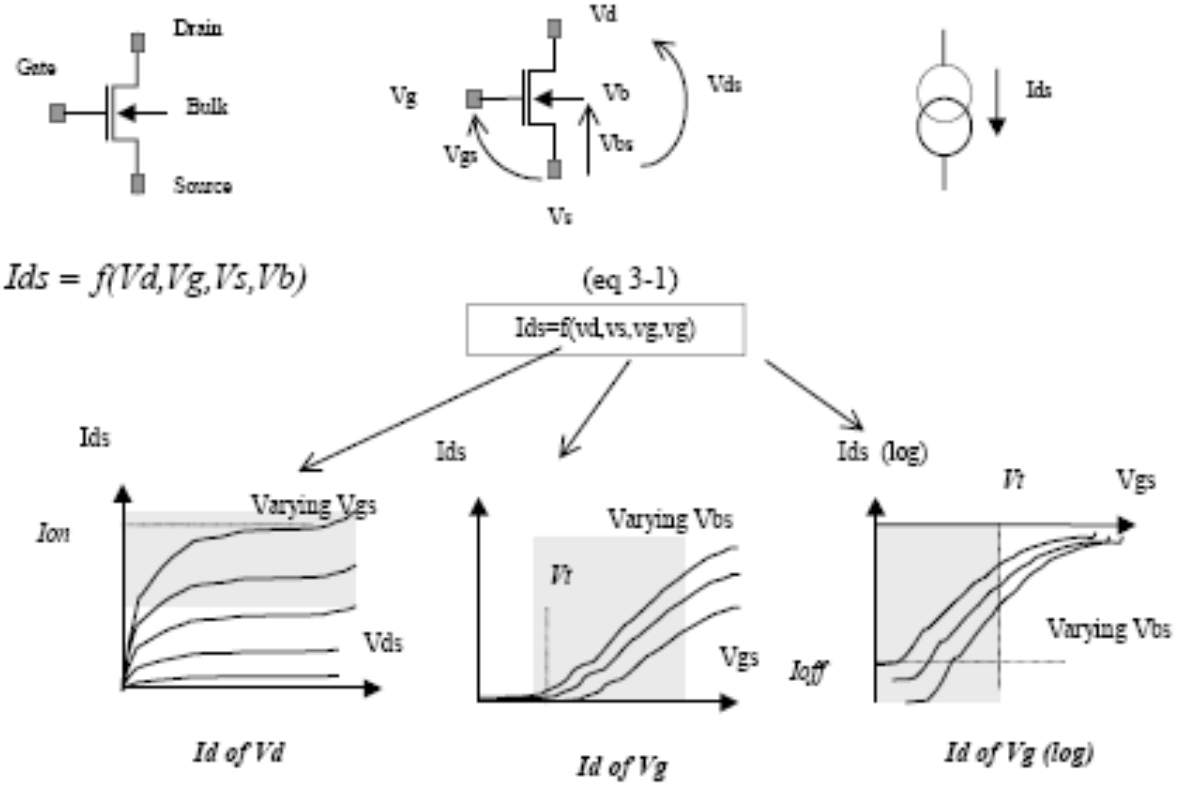
MOS transistor revisited (II)



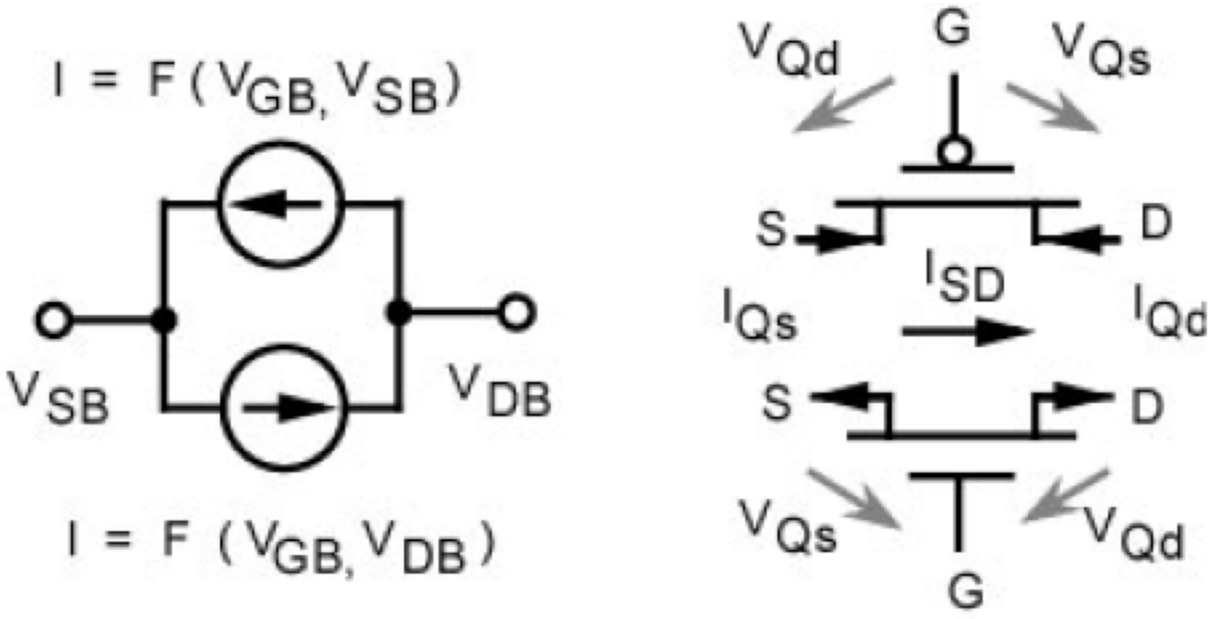
From: Introduction to VLSI Mead and Conway

MOS Transistor





SYMMETRIC MOS MODEL



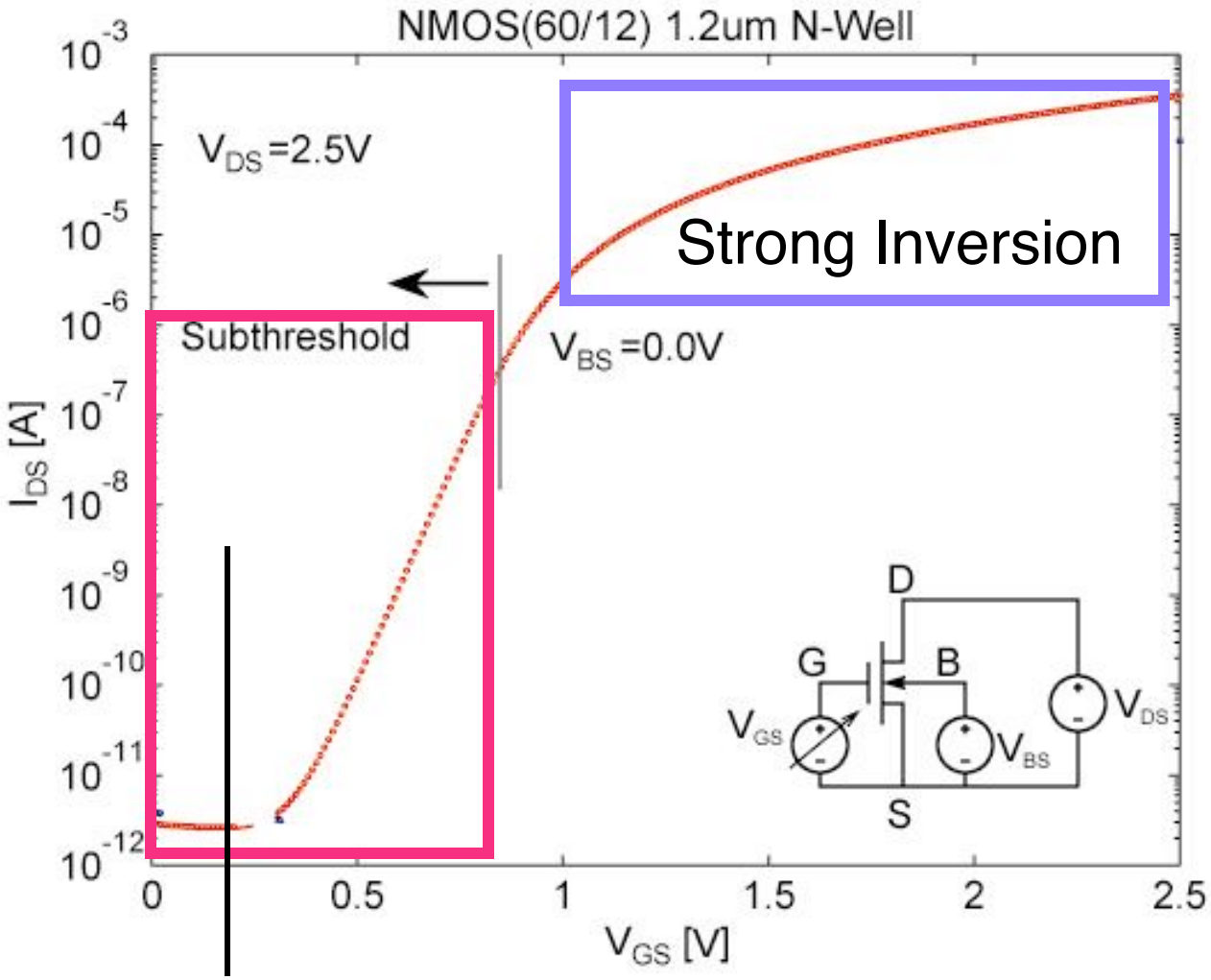
$$I_{SD} \propto F\left(V_{GB}, V_{SB}\right) - F\left(V_{GB}, V_{DB}\right)$$

WEAK INVERSION REGION

$$I_{SD} \propto G\left(V_{GB}\right)\left[H\left(V_{SB}\right) - H\left(V_{DB}\right)\right]$$

Weak (vs) Strong Inversion

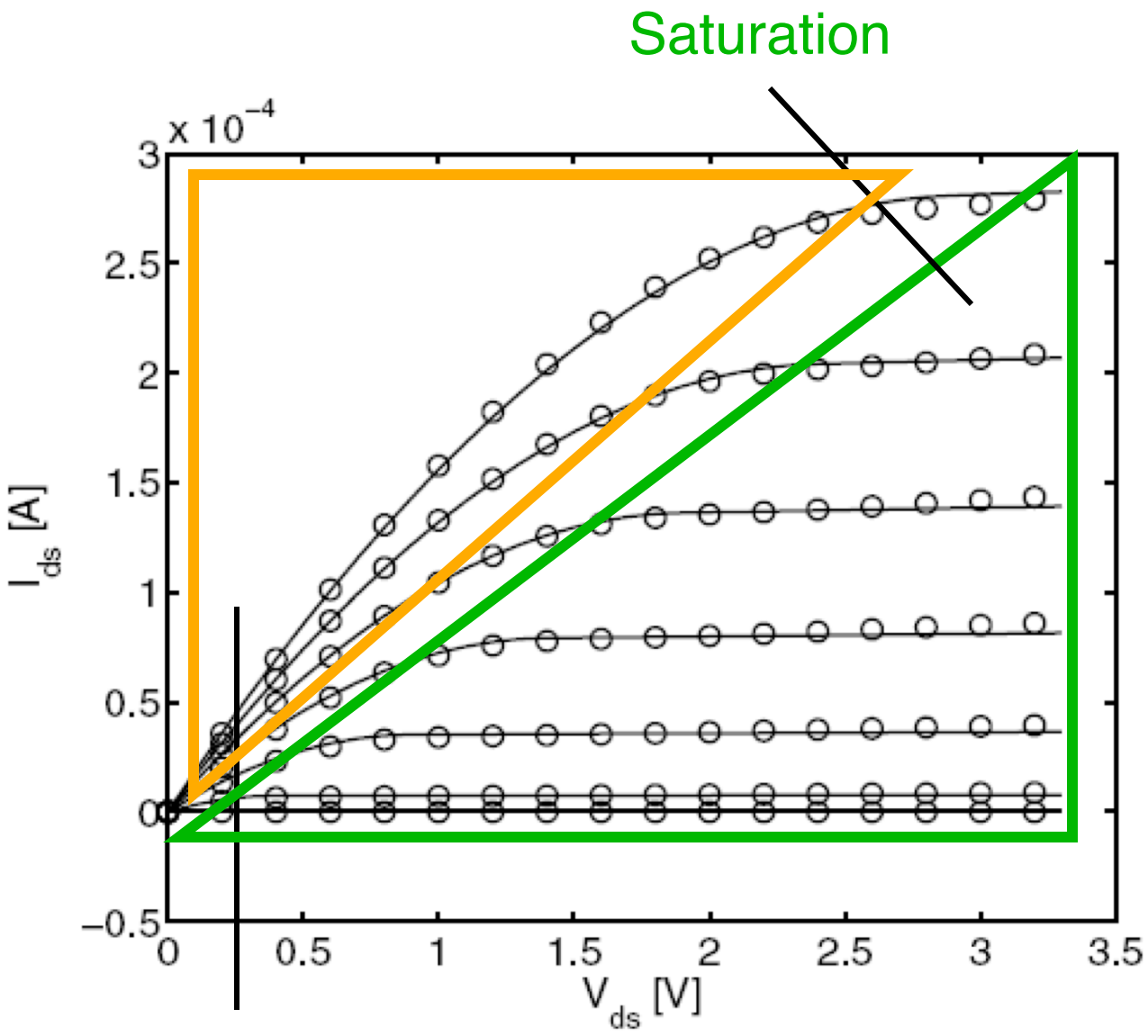
Device operation characterized by the form of the current as a function of the bias voltage between the gate and the source terminals (Vgs)



Weak Inversion (also known as Subthreshold)

Conduction (vs) Saturation

Device operation characterized by the form of the current as a function of the bias voltage between the DRAIN and the source terminals (Vds)



Conduction (also known as Ohmic)

MOS Model (above threshold): simple and non-symmetric!

$$If \quad V_{GS} < 0$$
$$I_{DS} = 0$$

$$If \quad V_{DS} > V_{GS} - V_{TO}$$
$$I_{DS} = \left(\frac{W}{L}\right)\left(\frac{UO}{2}\right)\frac{\varepsilon_0 \varepsilon_r}{TOX}\left(V_{GS} - V_T\right)^2$$

$$If \quad V_{DS} < V_{GS} - V_{TO}$$
$$I_{DS} = \left(\frac{W}{L}\right) UO \frac{\varepsilon_0 \varepsilon_r}{TOX}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$V_T = V_{TO} + GAMMA\left(\sqrt{PHI - V_{BS}} - \sqrt{PHI}\right)$$

$\varepsilon_0 = 8.85\ 10^{-12}$ F/m is the absolute permittivity

ε_r = relative permittivity, equal to 3.9 in the case of SiO2 (no unit)

Mos Model 1 parameters			
Parameter	Definition	Typical Value 0.12µm NMOS	PMOS
VTO	Theshold voltage	0.4V	-0.4V
U0	Carrier mobility	0.06m^2/V-s	0.02m^2/V-s
TOX	Gate oxide thickness	2nm	2nm
PHI	Surface potential at strong inversion	0.3V	0.3V
GAMMA	Bulk threshold parameter	0.4 V$^{0.5}$	0.4 V$^{0.5}$
W	MOS channel width	1µm	1µm
L	MOS channel length	0.12µm	0.12µm

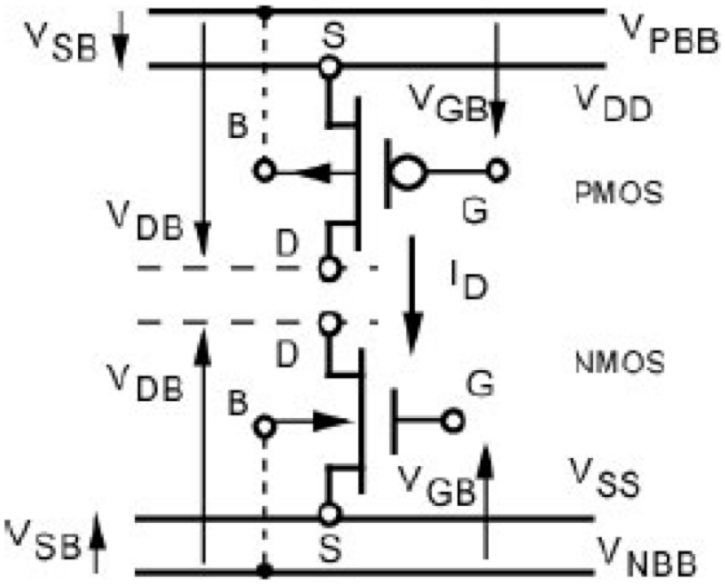
MOS Model (sub-threshold)

NMOS

$$I_D \equiv I_{DS} = S\, I_{n0} \exp\left(\frac{\kappa_n V_{GB}}{V_t}\right)\left[\exp\left(\frac{-V_{SB}}{V_t}\right) - \exp\left(\frac{-V_{DB}}{V_t}\right)\right]$$

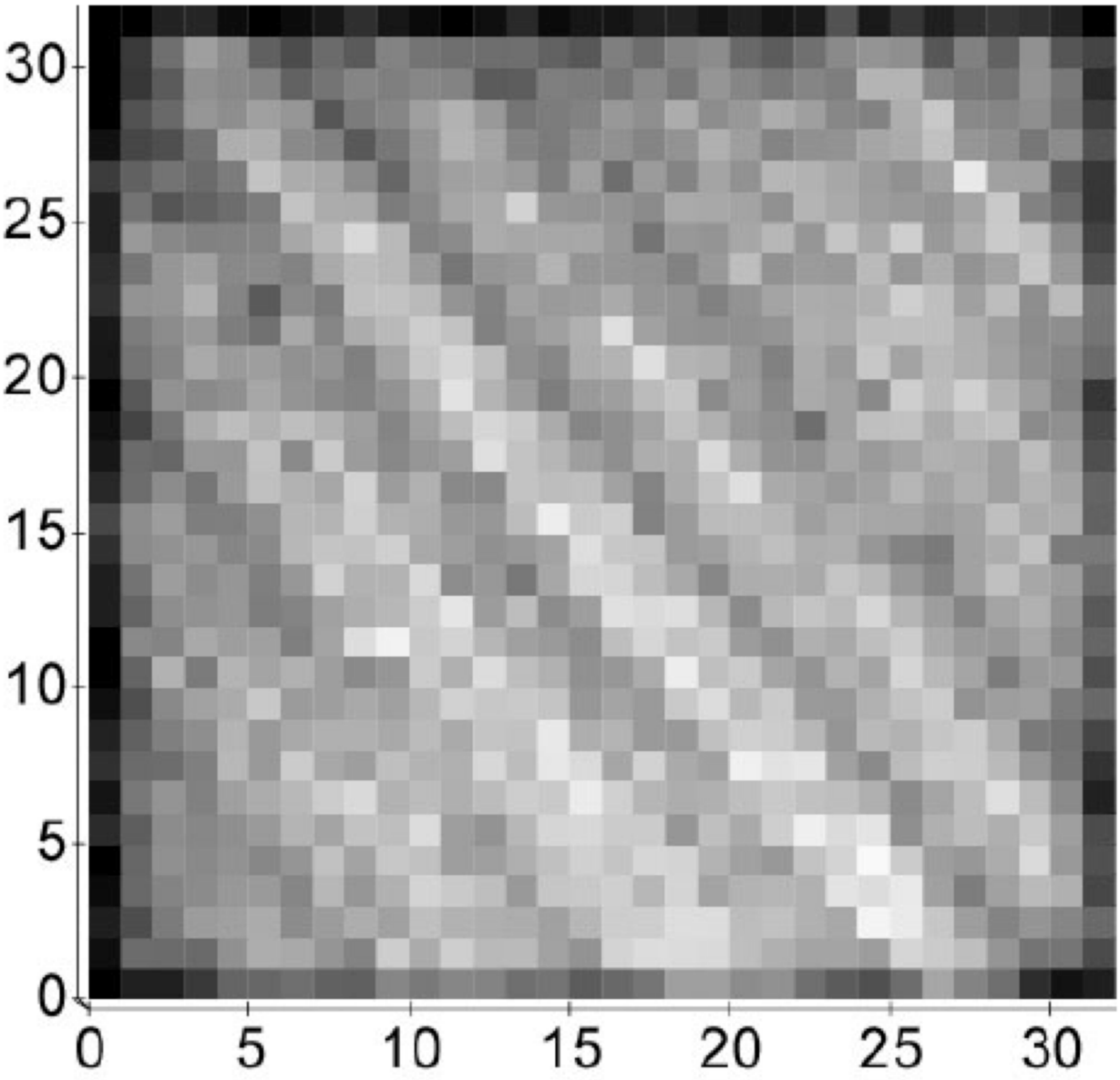
PMOS

$$I_D \equiv I_{SD} = S\, I_{p0} \exp\left(\frac{-\kappa_p V_{GB}}{V_t}\right)\left[\exp\left(\frac{V_{SB}}{V_t}\right) - \exp\left(\frac{V_{DB}}{V_t}\right)\right]$$

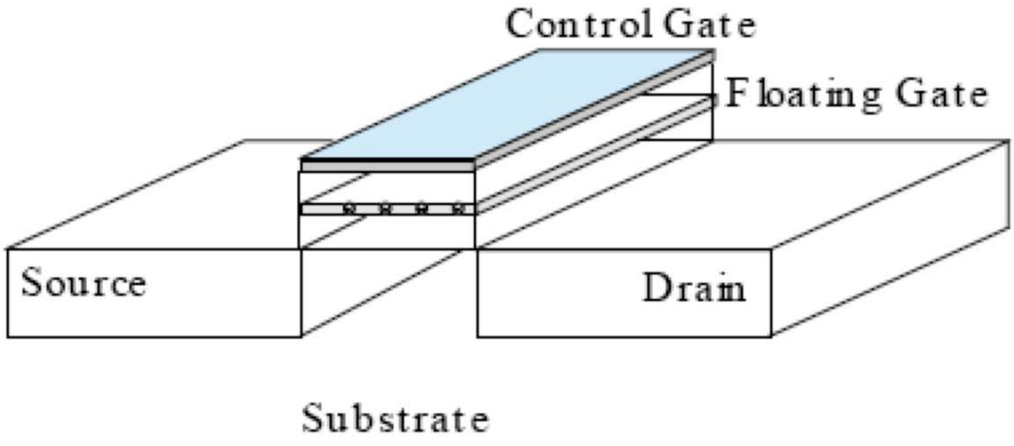


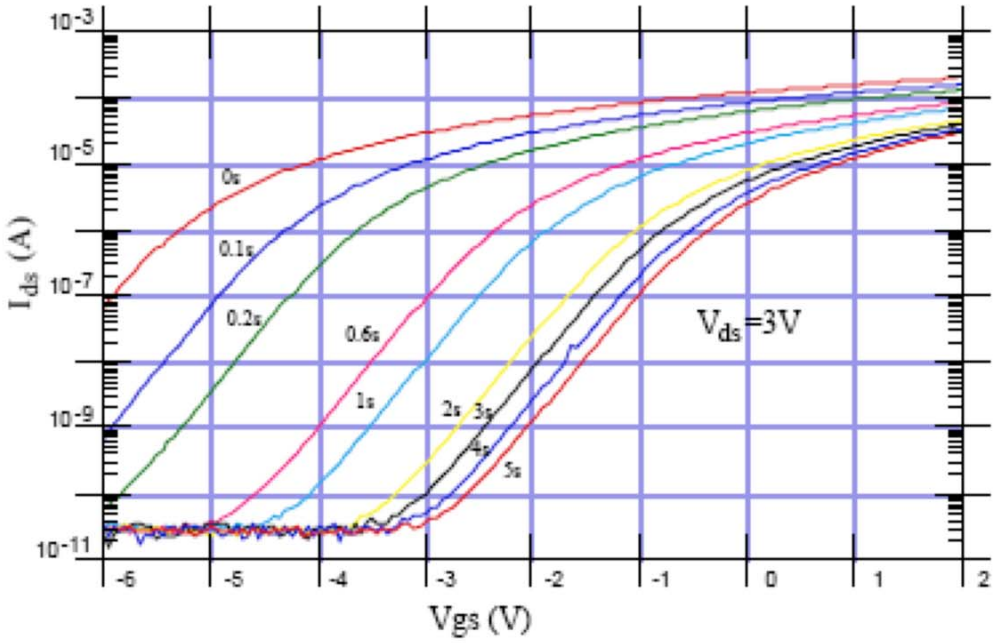
$$V_t \equiv \frac{kT}{q} \qquad \kappa \equiv \frac{1}{\eta} \equiv \frac{C_{ox}}{C_{ox} + C_{dep}} \qquad S = \frac{W}{L}$$

MOS MISMATCH



FLOATING GATE MOS (FGMOS)

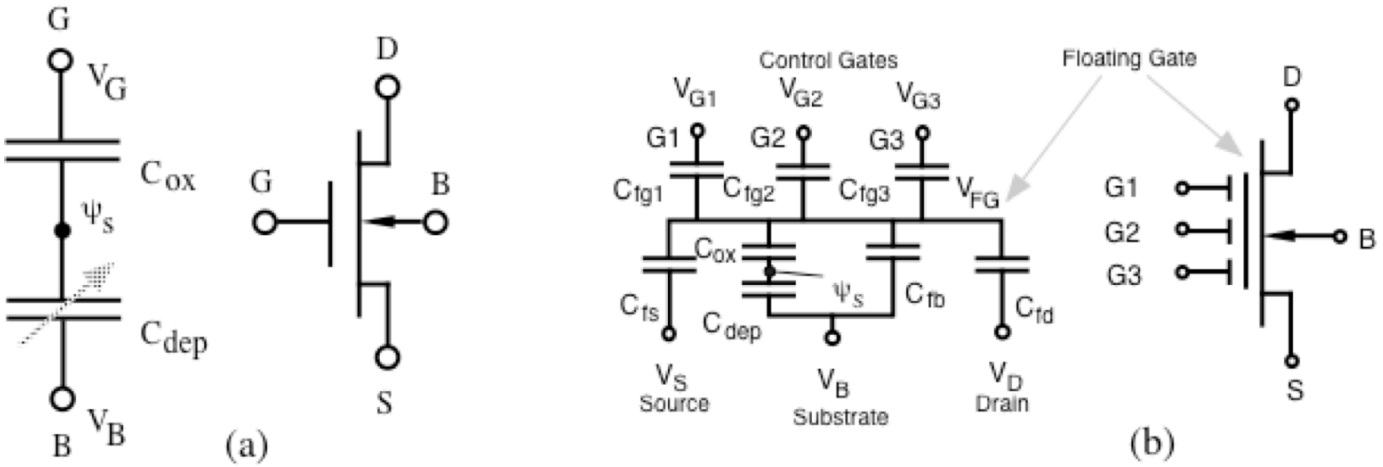




MOS CAPACITANCE MODEL

MOS

FGMOS



$$V_{FG_i} = \frac{Q_{FG_i}}{C_{T_i}} + \sum_{j=1}^{N} \Lambda_{ij} V_{G_j}$$

$$\Lambda_{ij} = \frac{C_{fg}}{C_{T_i}}$$