# Lecture 8
# Local and Global Interconnects

# Modeling Interconnects – capacitance of a single wire-

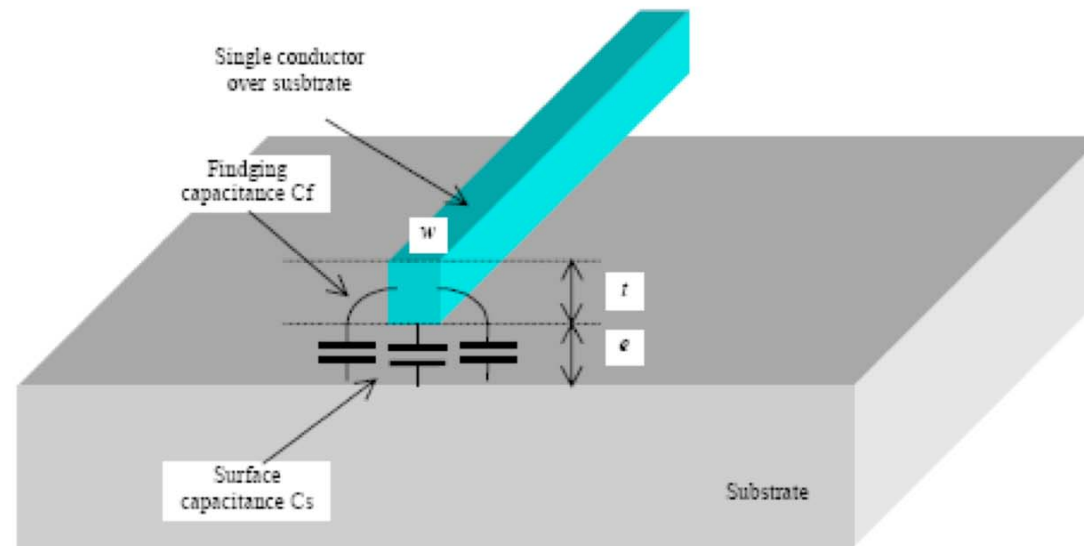



*Figure 5-18: One conductor above a ground plane*

$$C = C_s + 2.C_f \;=\; \varepsilon_0 \varepsilon_r (1{,}13.\frac{w}{e} + 1{,}44.(\frac{w}{e})^{0{,}11} + 1{,}46.(\frac{t}{e})^{0{,}42}) \qquad (5\text{-}2)$$

C = total capacitance per meter (Farad/m)

Cs= surface capacitance (Farad/meter)

Cf = fringing capacitance (Farad/m)

$\varepsilon_0$ = 8.85 e $^{-12}$ Farad/m

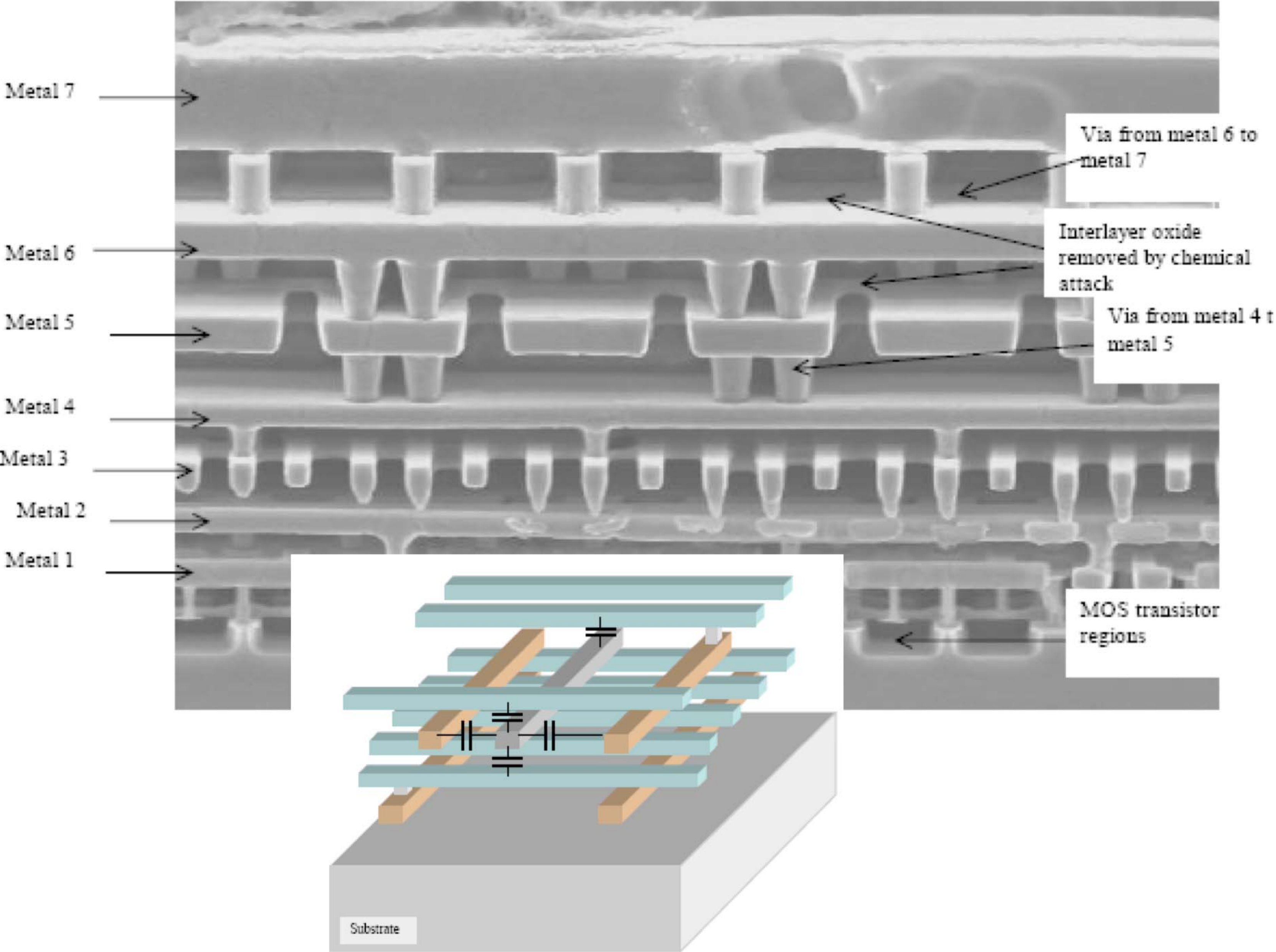
$\varepsilon_r$ = 3.9 for $SiO_2$

w= conductor width (m)

t= conductor thickness (m)

e = dielectric thickness (m)

# wires everywhere!



# Modeling Interconnects – capacitance of two wires-

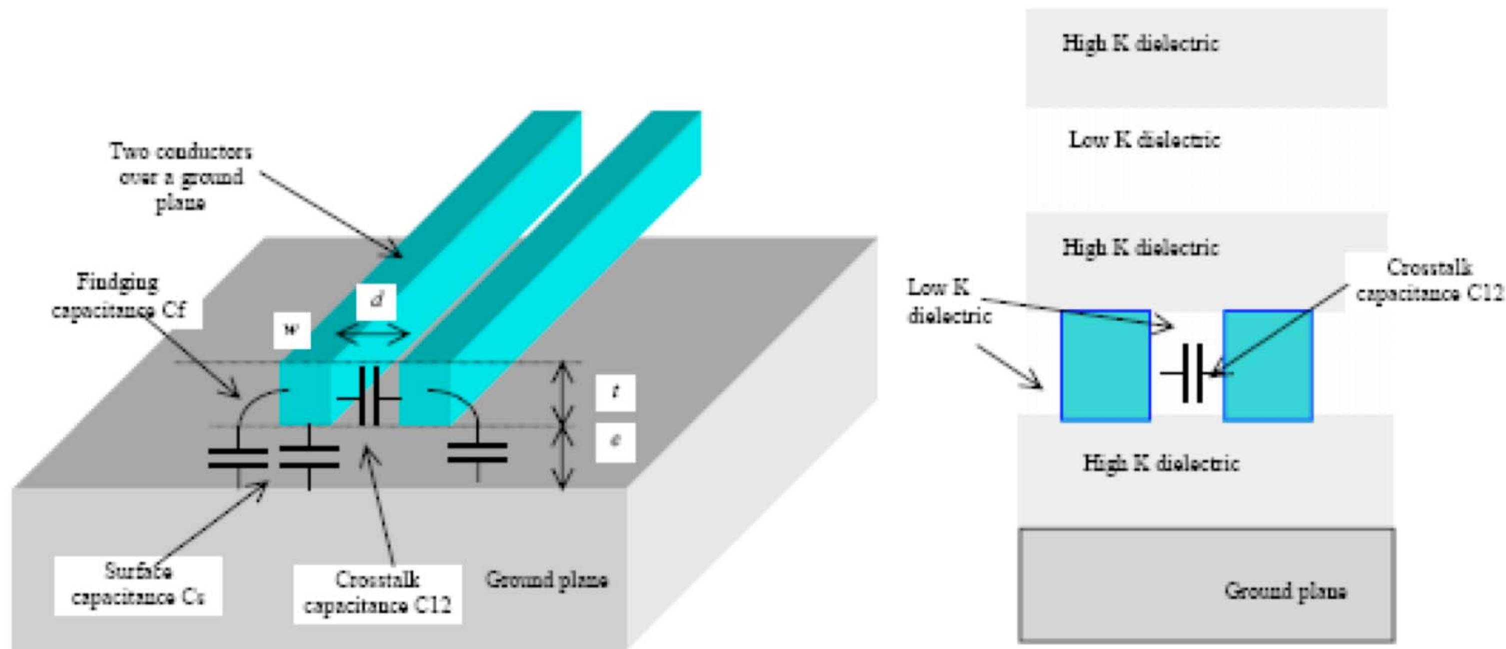



*Figure 5-20: Two conductors above a ground plane*

$$C = C_s + C_f = \varepsilon_0 \varepsilon_r (1.10\frac{w}{e} + 0.79(\frac{w}{e})^{0.1} + 0.46.(\frac{t}{e})^{0.17}(1-0.87e^{(\frac{-d}{e})})) \qquad (5\text{-}3)$$

$$C_{12} = \varepsilon_0 \varepsilon_{rlowK}(\frac{t}{d} + 1.2(\frac{d}{e})^{0.1}.(\frac{d}{e}+1.15)^{-2.22} + 0.253\ln(1+7.17\frac{w}{d}).(\frac{d}{e}+0.54)^{-0.64}) \qquad (5\text{-}4)$$

C = conductor capacitance to ground per meter (Farad/m)

Cs= surface capacitance (Farad/meter)

# Modeling Interconnects –layout capacitance example-

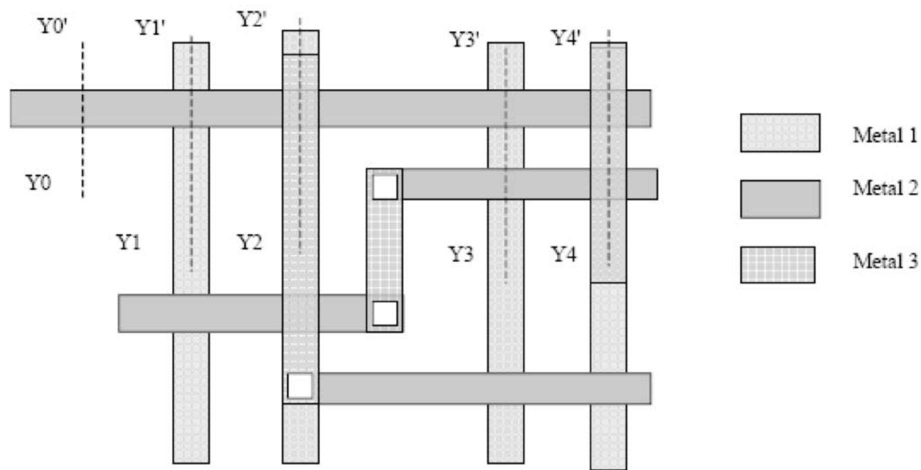
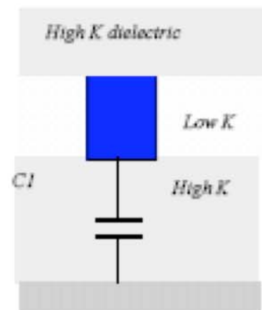
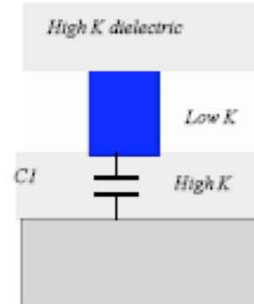



*Figure 5-21: Example of interconnects routed in metal 1, 2 and 3*



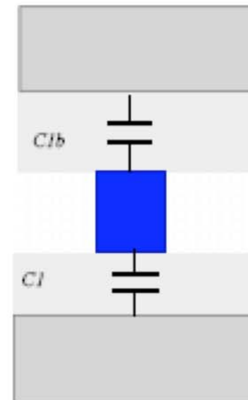

*One conductor above substrate (Y0-Y0')*

C=C1=70fF/mm



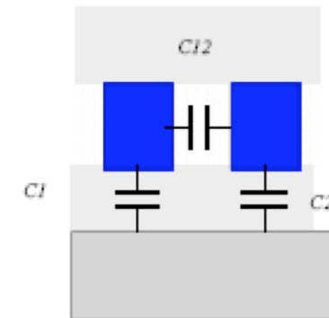

*One conductor, one plane (Y1-Y1')*

C=C1=120fF/mm




*One conductor, two planes (Y2-Y2')*

C=C1+C1b=150fF/mm




*Two conductors, one plane (Y3-Y3')*

C=C1 =90fF/mm
C12 = 50fF/mm

# Interconnect resistance

| | | | |
|---|---|---|---|
| $\rho_{Ag}$ | Gold resistivity | Bonding between chip and package | $2.20\ 10^{-6}\ \Omega.cm$ |
| $\rho_{tungsten}$ | Tungsten resistivity | Contacts | $5.30\ 10^{-6}\ \Omega.cm$ |
| $\rho_{Ndiff}$ | Highly doped silicon resistivity | N+ diffusions | $0.25\ \Omega.cm$ |
| $\rho_{Nwell}$ | Lightly doped silicon resistivity | N well | $50\ \Omega.cm$ |
| $\rho_{si}$ | Intrinsic silicon resistivity | Substrate | $2.5\ 10^{5}\ \Omega.cm$ |

*Table 5-3: Resistivity of several materials used in CMOS circuits*

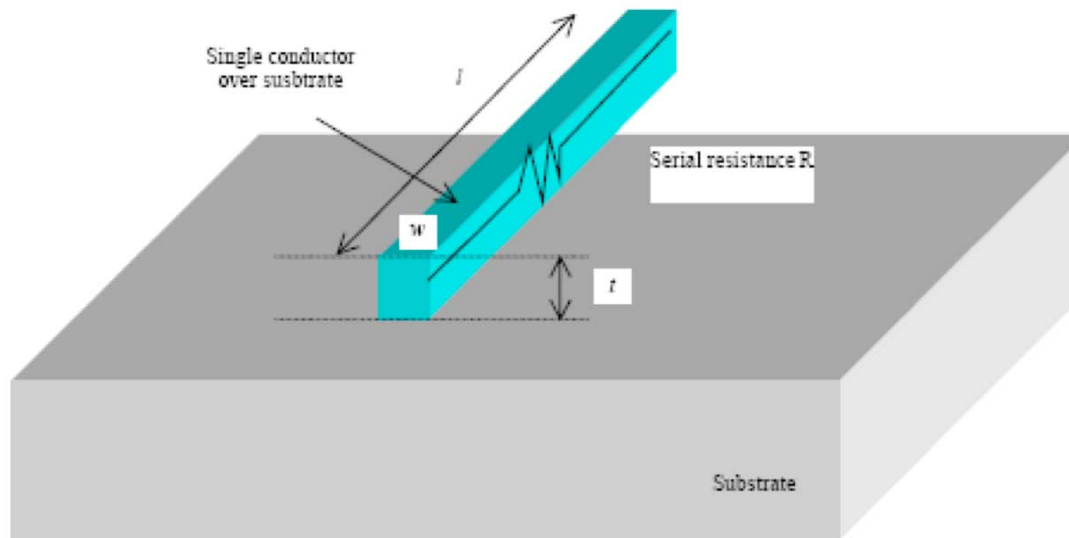



*Figure 5-26: Resistance of a conductor*

$$R = \rho \frac{l}{w.t} \qquad \text{(Equ. 5-5)}$$

where

R=serial resistance (ohm)

ρ=resistivity (ohm.m)

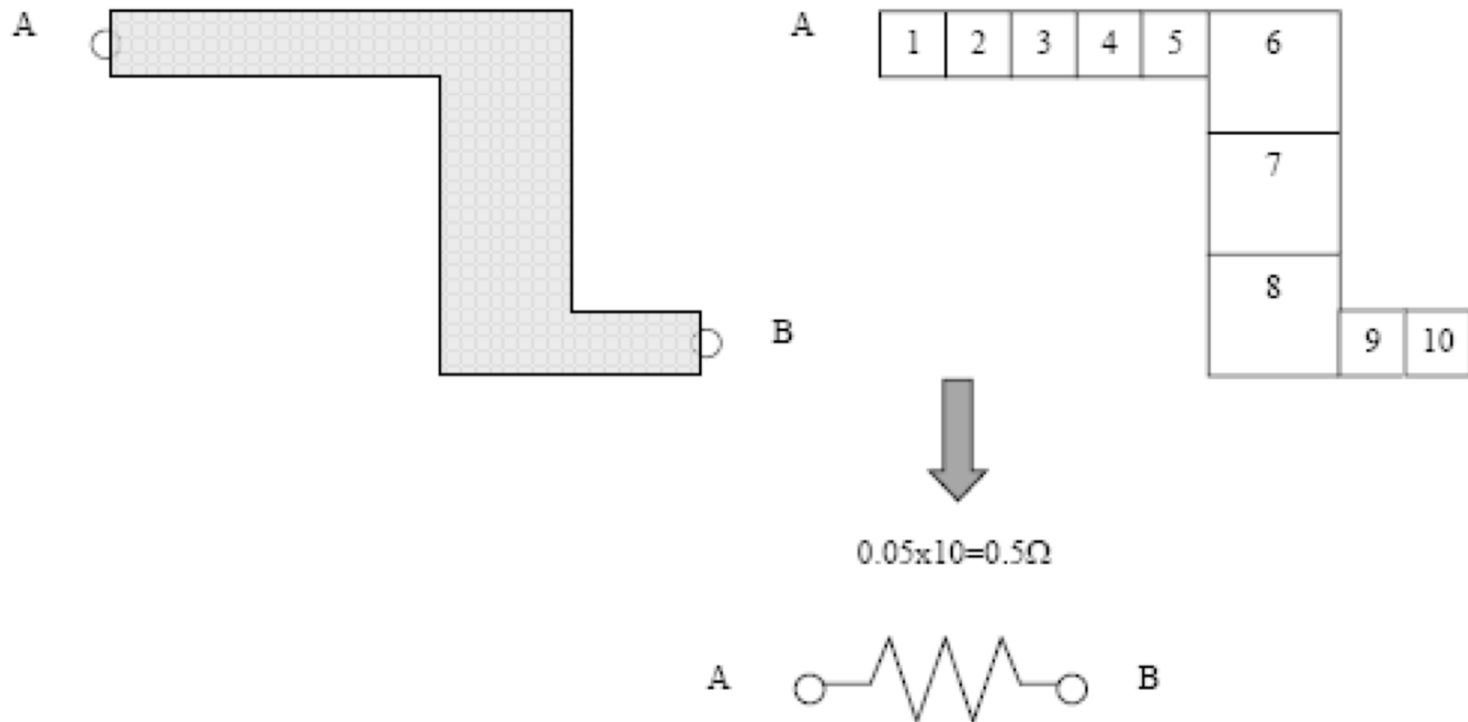
w= conductor width (m)

t= conductor thickness (m)

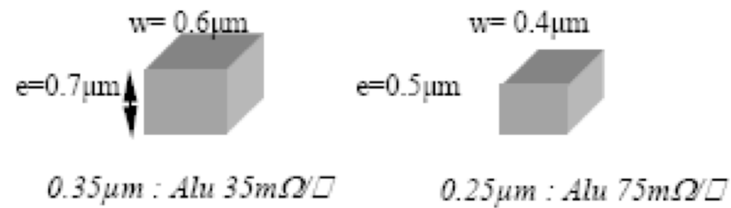
l = conductor length (m)

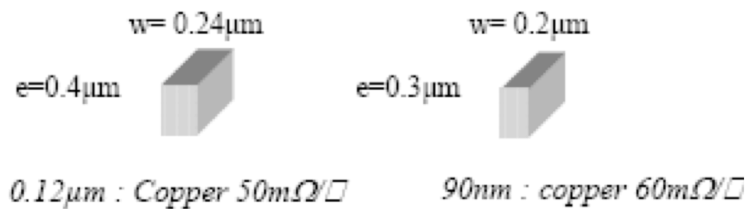
d = conductor distance (m)

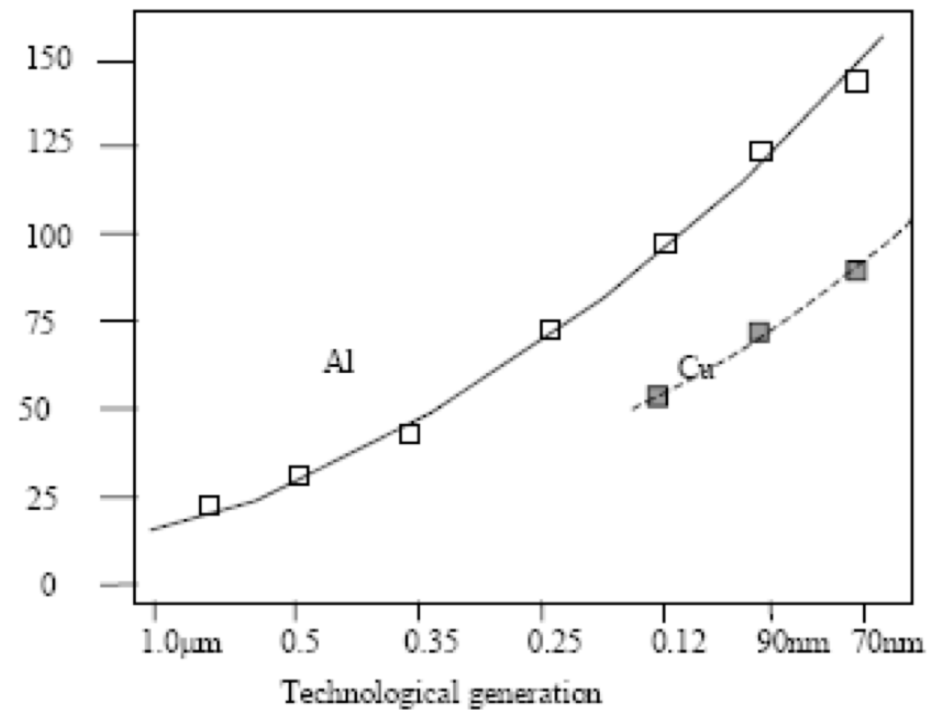
# Estimating resistance of a wire –measuring squares-



# Interconnect resistance scaling

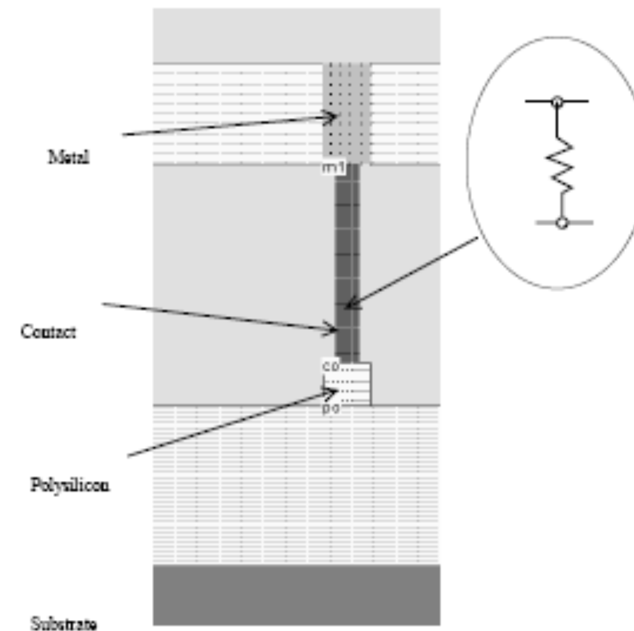


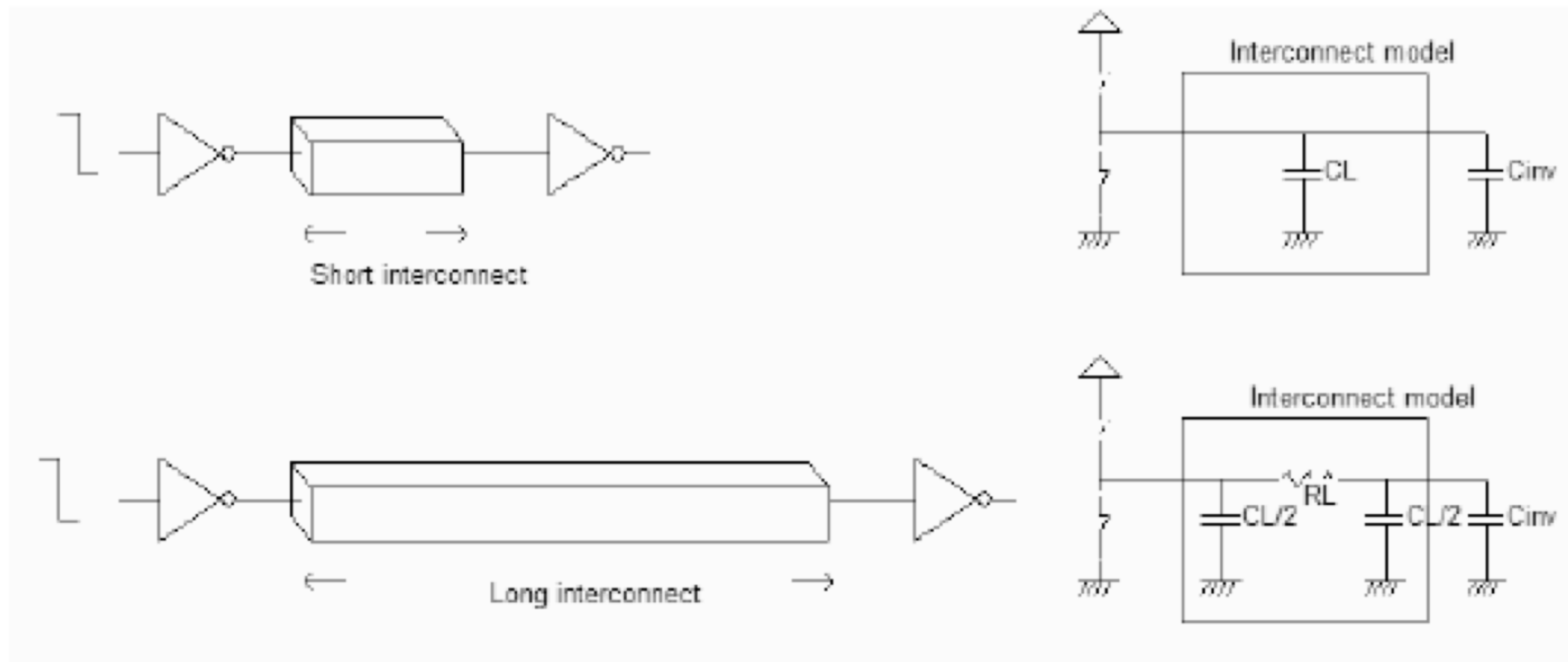
# Via resistance

| Technology | 0.7µm | 0.12µm | 90nm |
| --- | --- | --- | --- |
| Contact resistance | 0.5 Ω | 15 Ω | 20 Ω |
| Via | 0.3 Ω | 4 Ω | 8 Ω |
| Upper via | - | 1 Ω | 3 Ω |



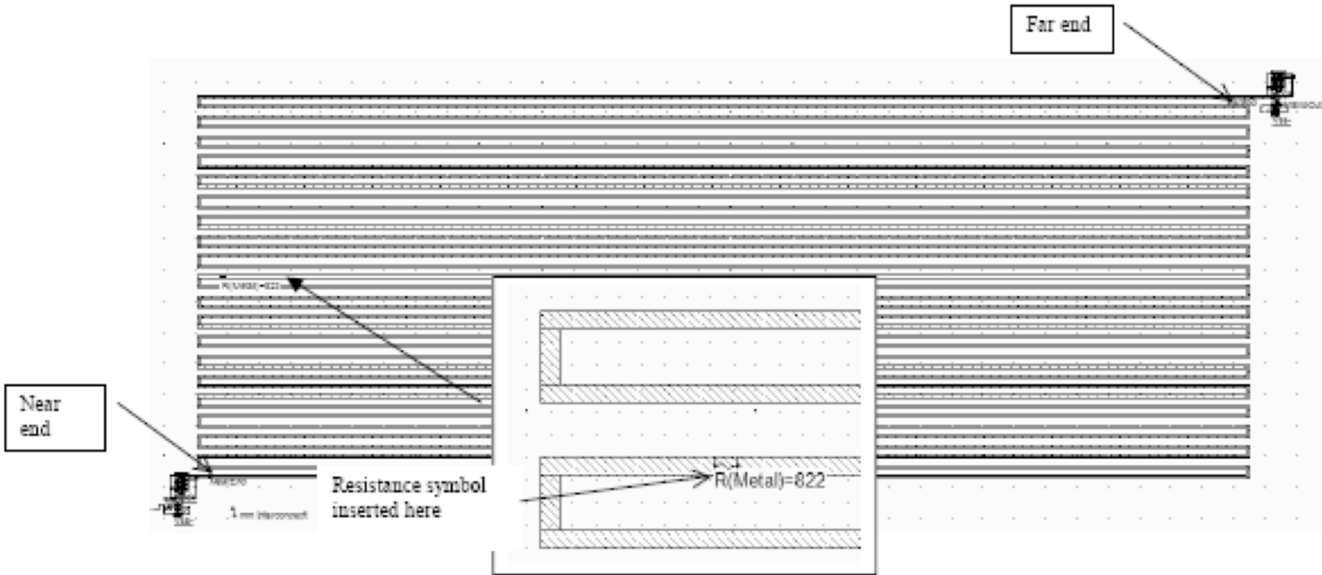
# Modeling interconnects

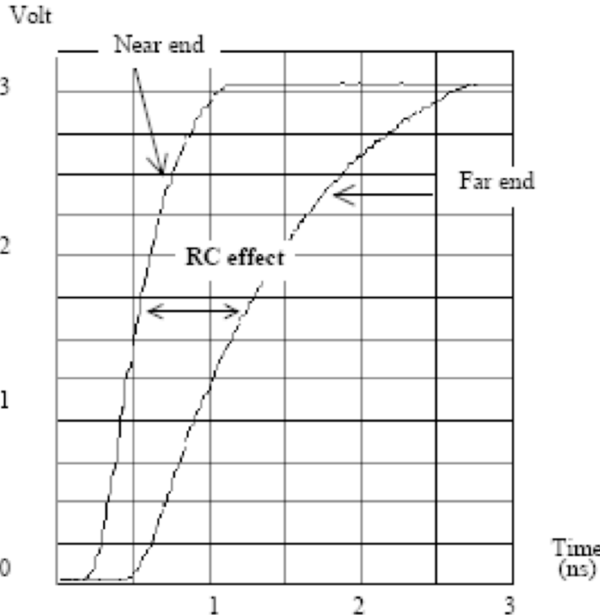
Lumped parameter: (C)




Distributed: (R-C)

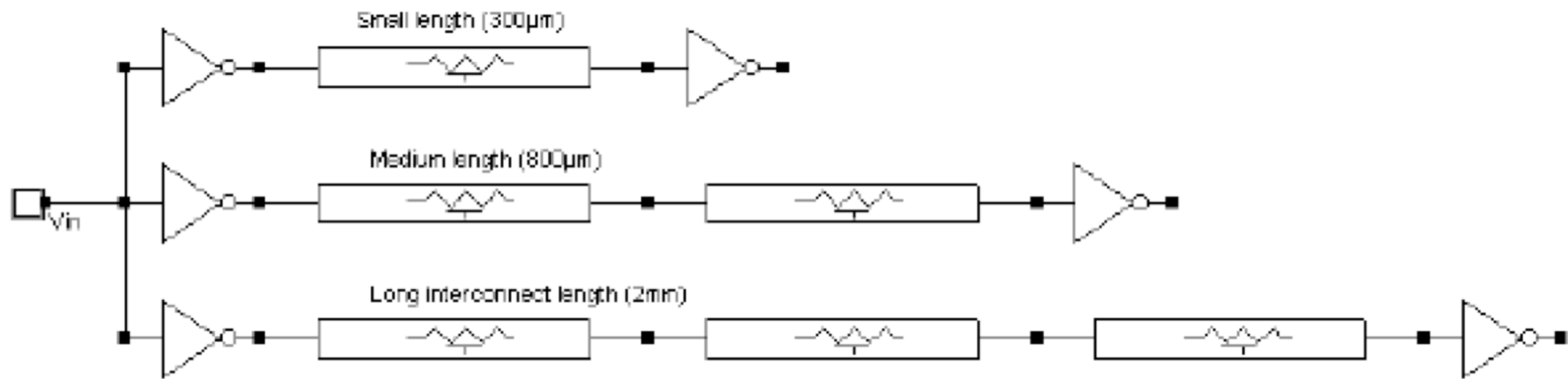
# Simulation




*(a) 10mm, metal 3, 0.35µm technology*

# Modeling interconnects (II)



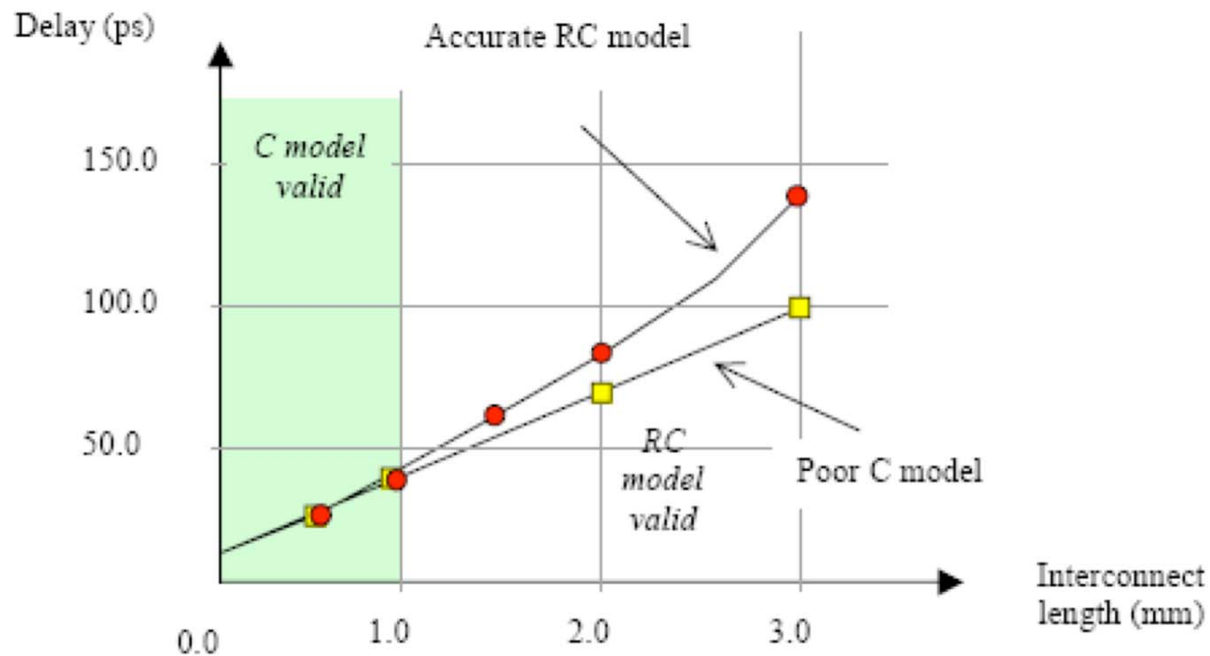
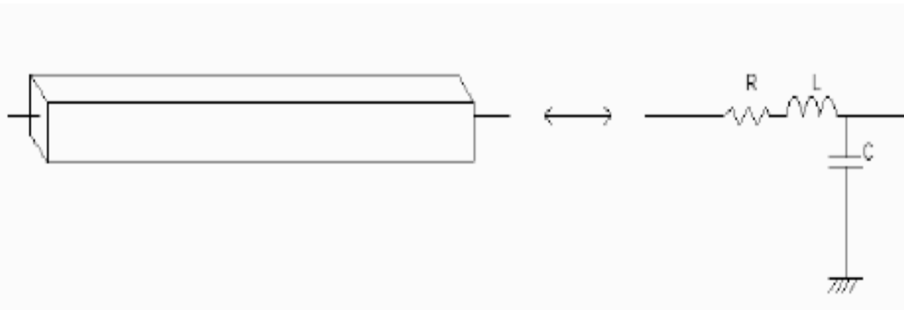
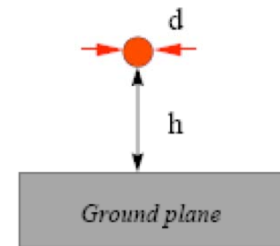




*Figure 5-43: Below 1mm, the C model is valid. Above 1mm, the RC model should be considered in 0.12µm CMOS technology*

# how about inductance?



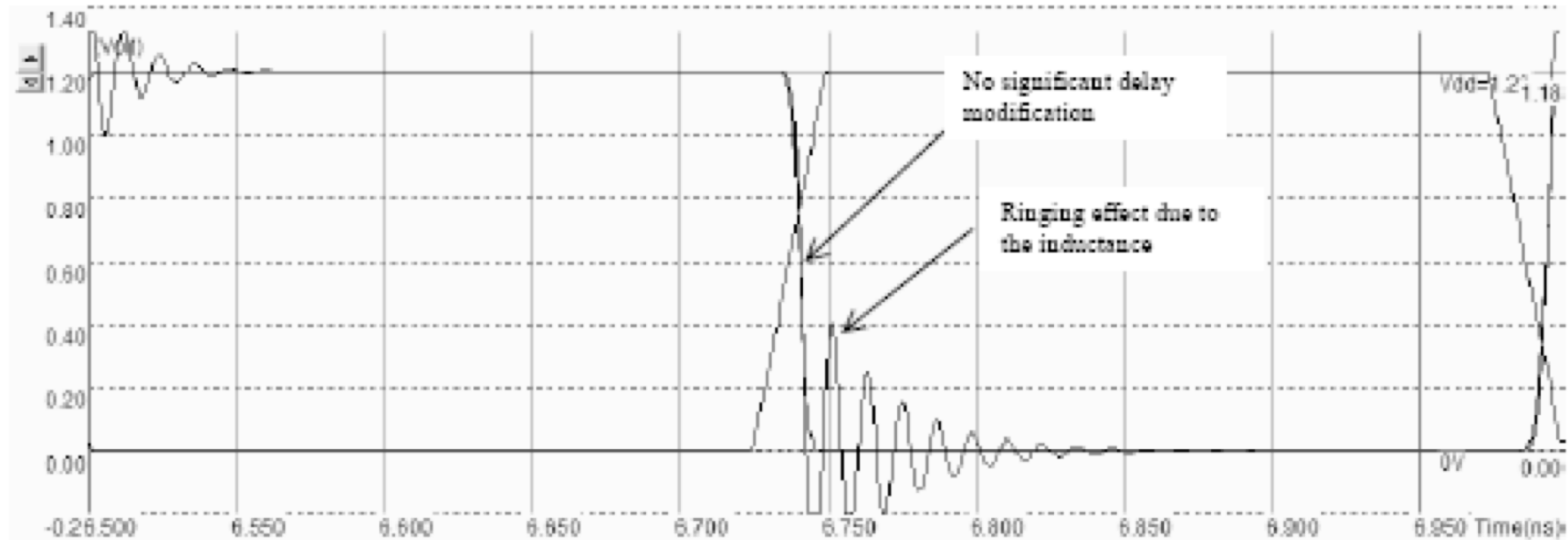

$$L = \frac{\mu 0}{2\pi} ln(4\frac{h}{d})$$ (Equ. 5-7)

with

$\mu_0$=1.257e$^{-6}$ H/m for most materials (Al, Cu, Si, $SiO_2$ and $Si_3N_4$)

d= wire diameter (m)

h = height of the wire vs. ground (m)



# transistor and interconnect models

## A Pair of Inverters