





The Digital Abstraction

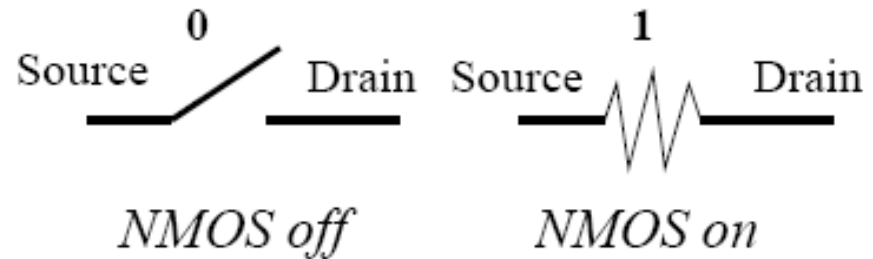
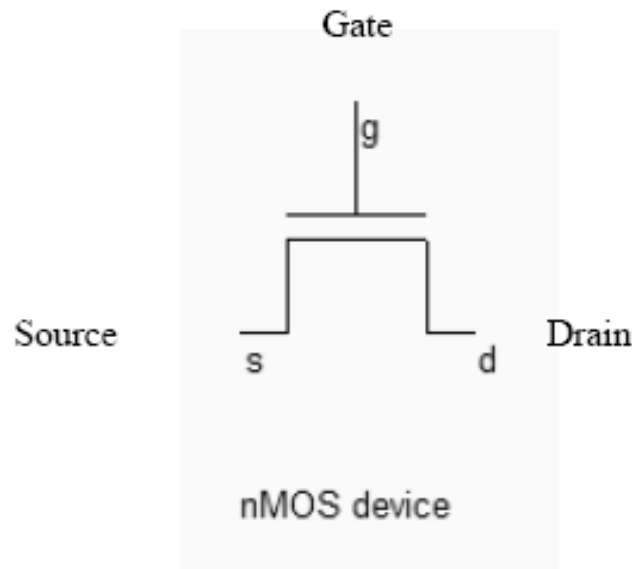
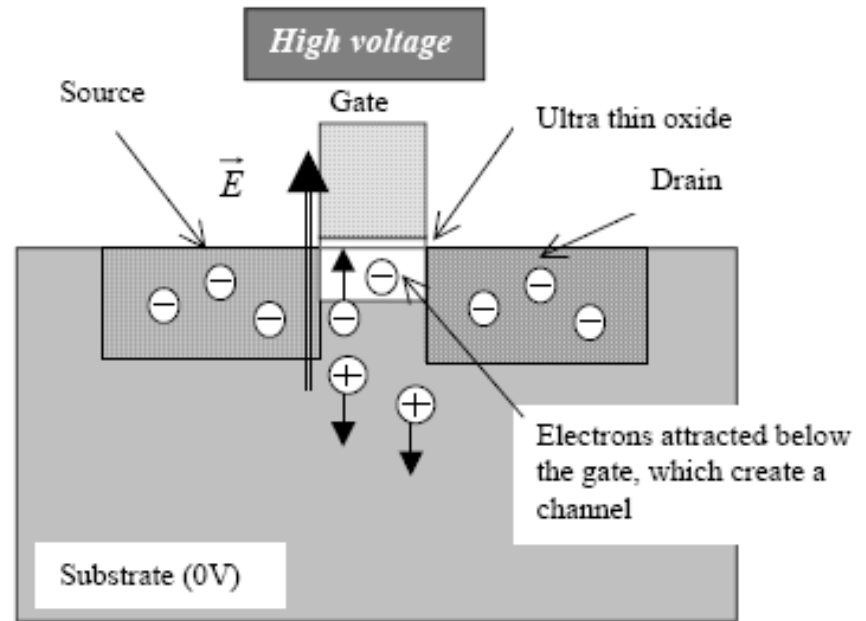
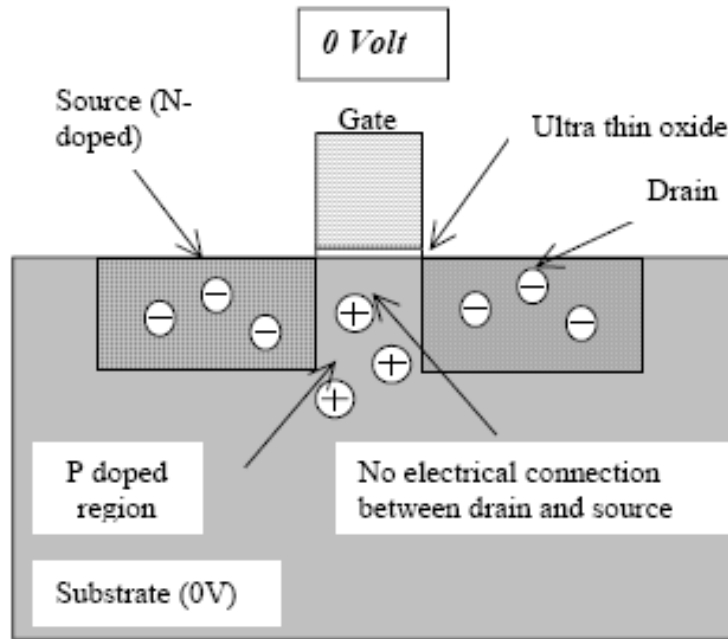
Andreas G. Andreou

where are we?

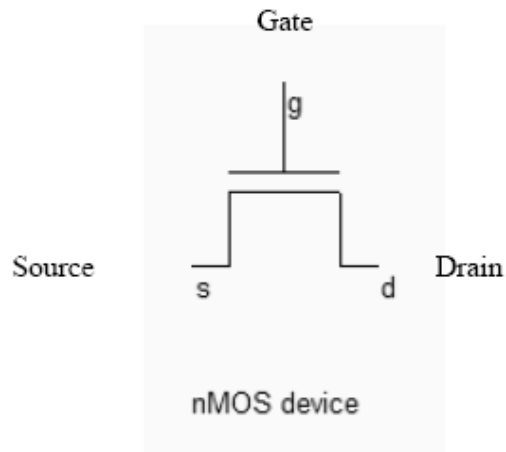
logic levels definitions

Logical value	Voltage	Name	Symbol in DSCH	Symbol in Microwind
0	0.0V	VSS	 (Green in logic simulation)	 (Green in analog simulation)
1	1.2V in cmos 0.12μm	VDD	 (Red in logic simulation)	 (Red in analog simulation)
X	Undefined	X	(Gray in simulation)	(Gray in simulation)

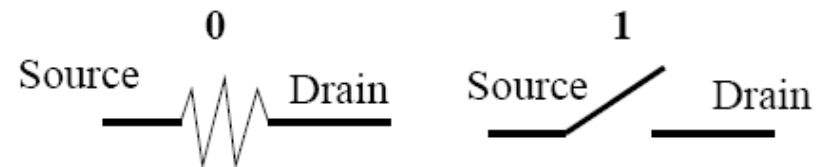
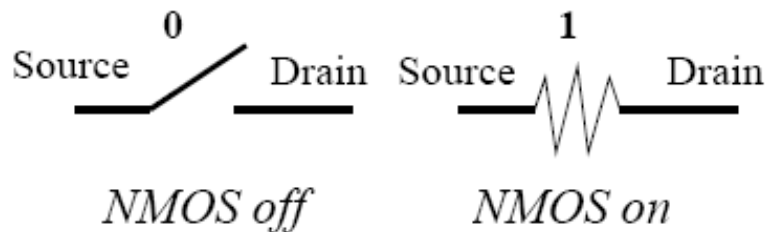
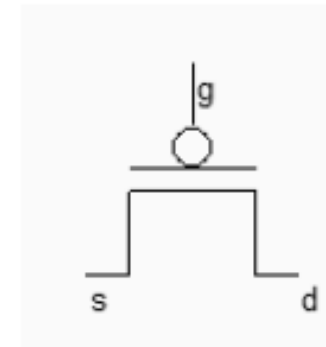
MOS transistor



NMOS and PMOS digital “models”



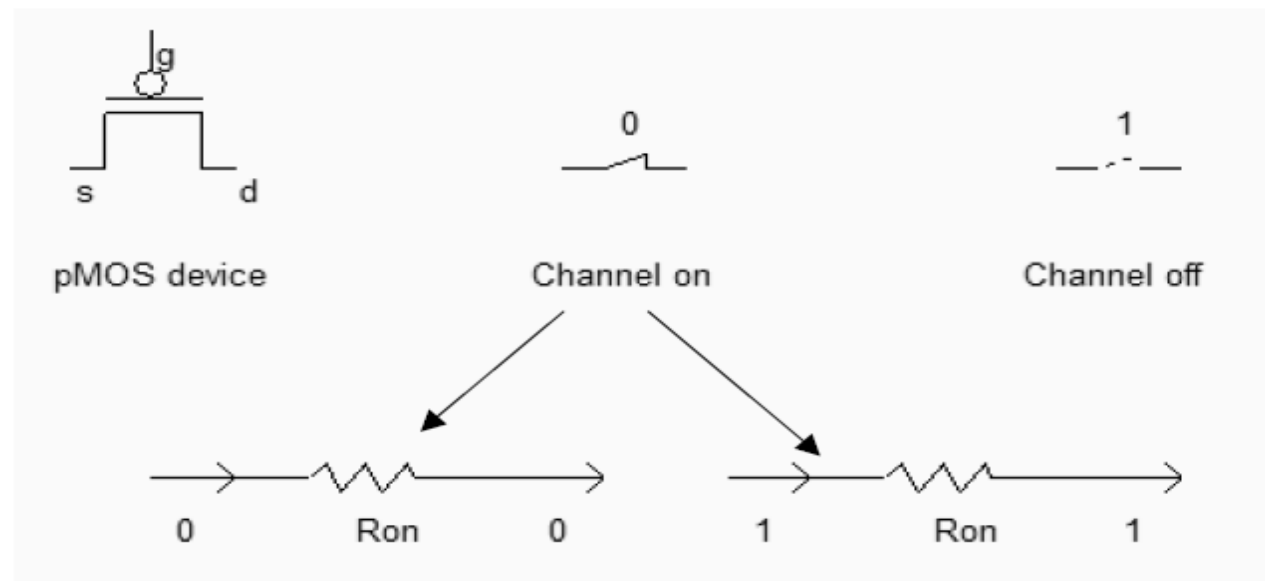
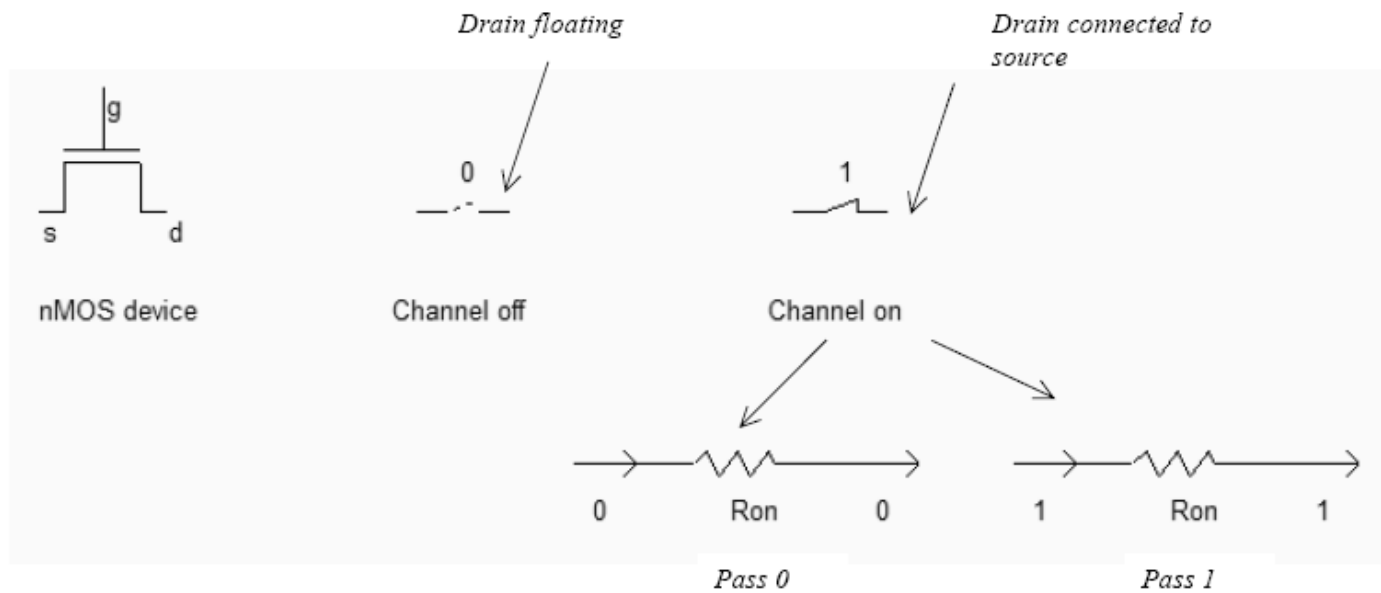
pMOS



Gate	Source	Drain
0	0	X
0	1	X
1	0	0
1	1	1

Gate	Source	Drain
0	0	0
0	1	1
1	0	X
1	1	X

what does this all mean?



and back to layout

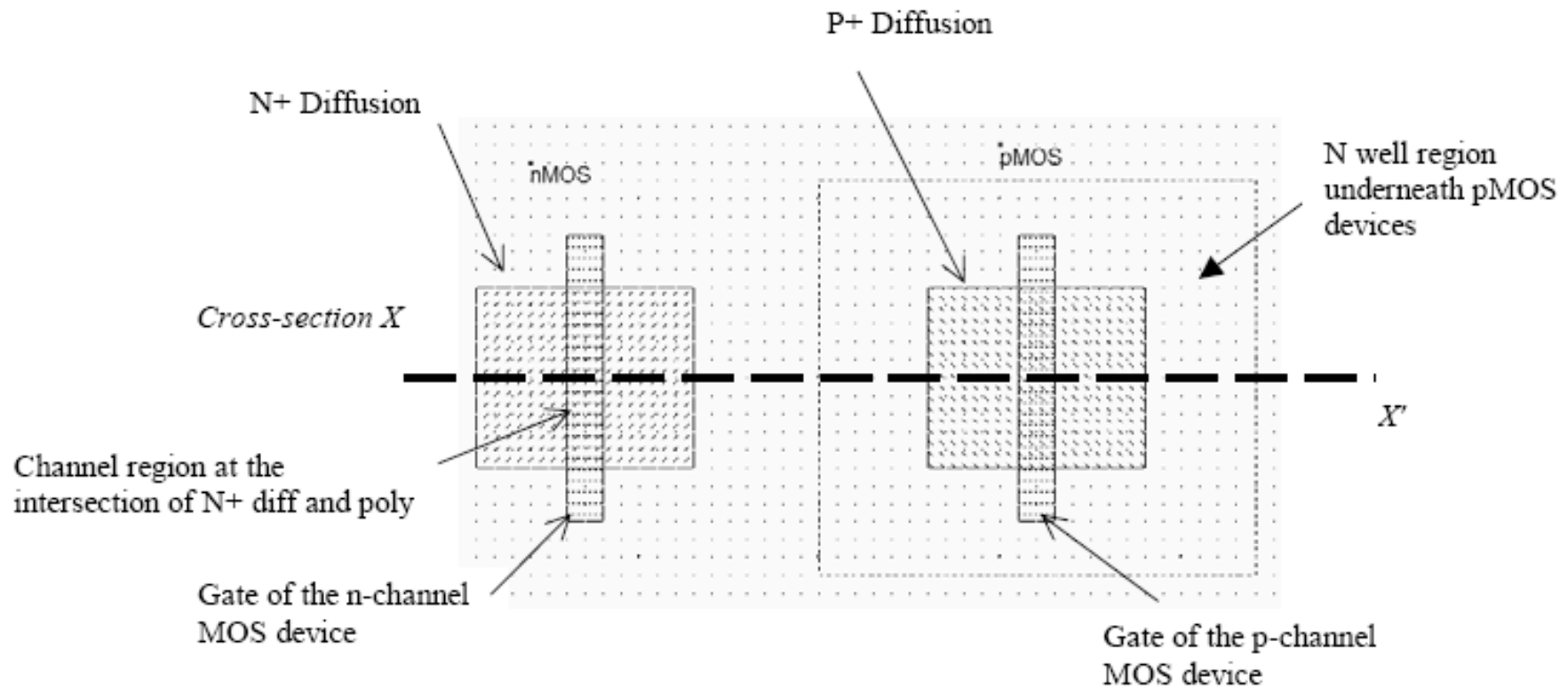


Figure 2-14: Bird's view of the n-channel and p-channel MOS device layout (*allMosDevices.MSK*)

cross-section and zoom

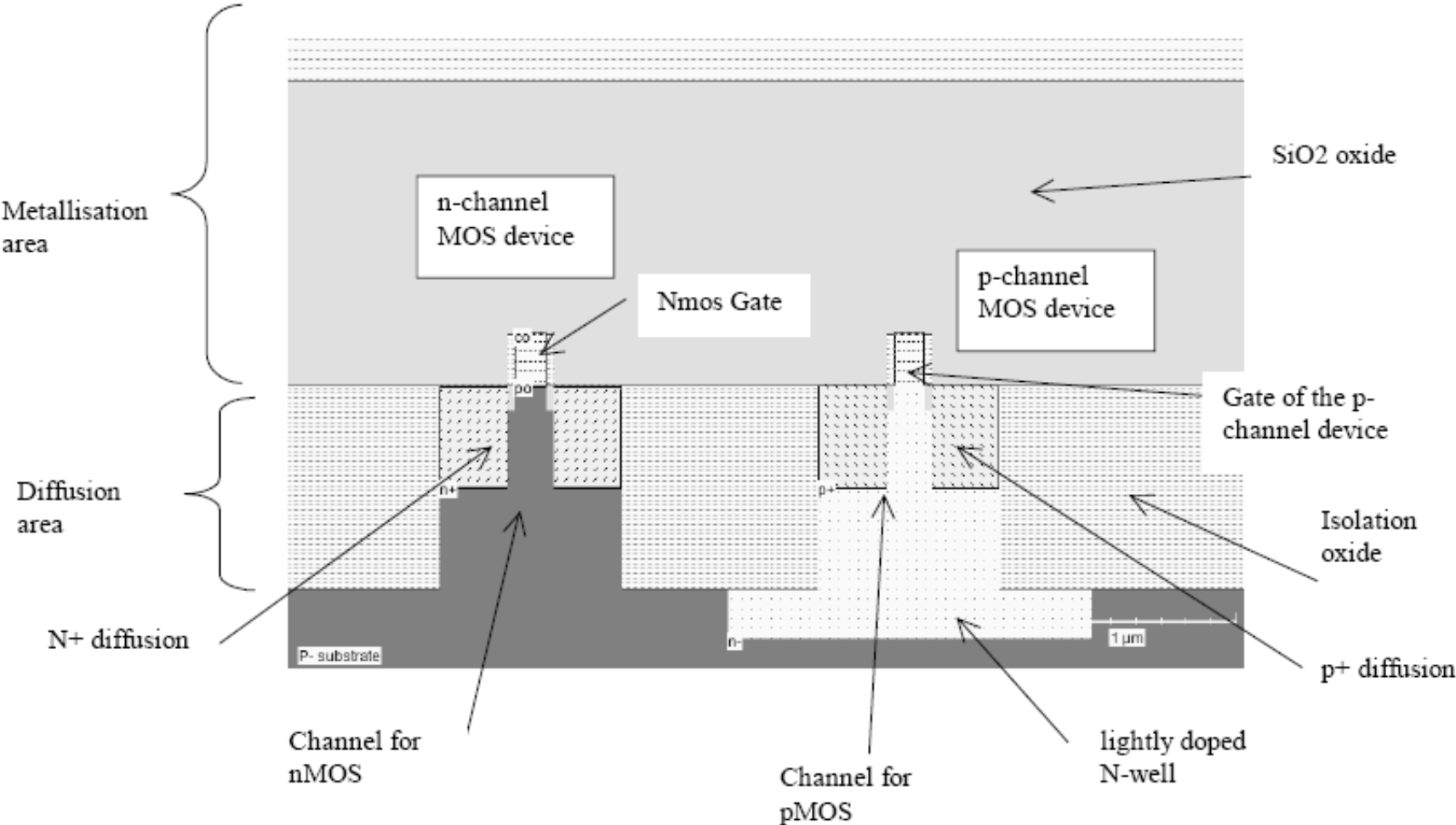
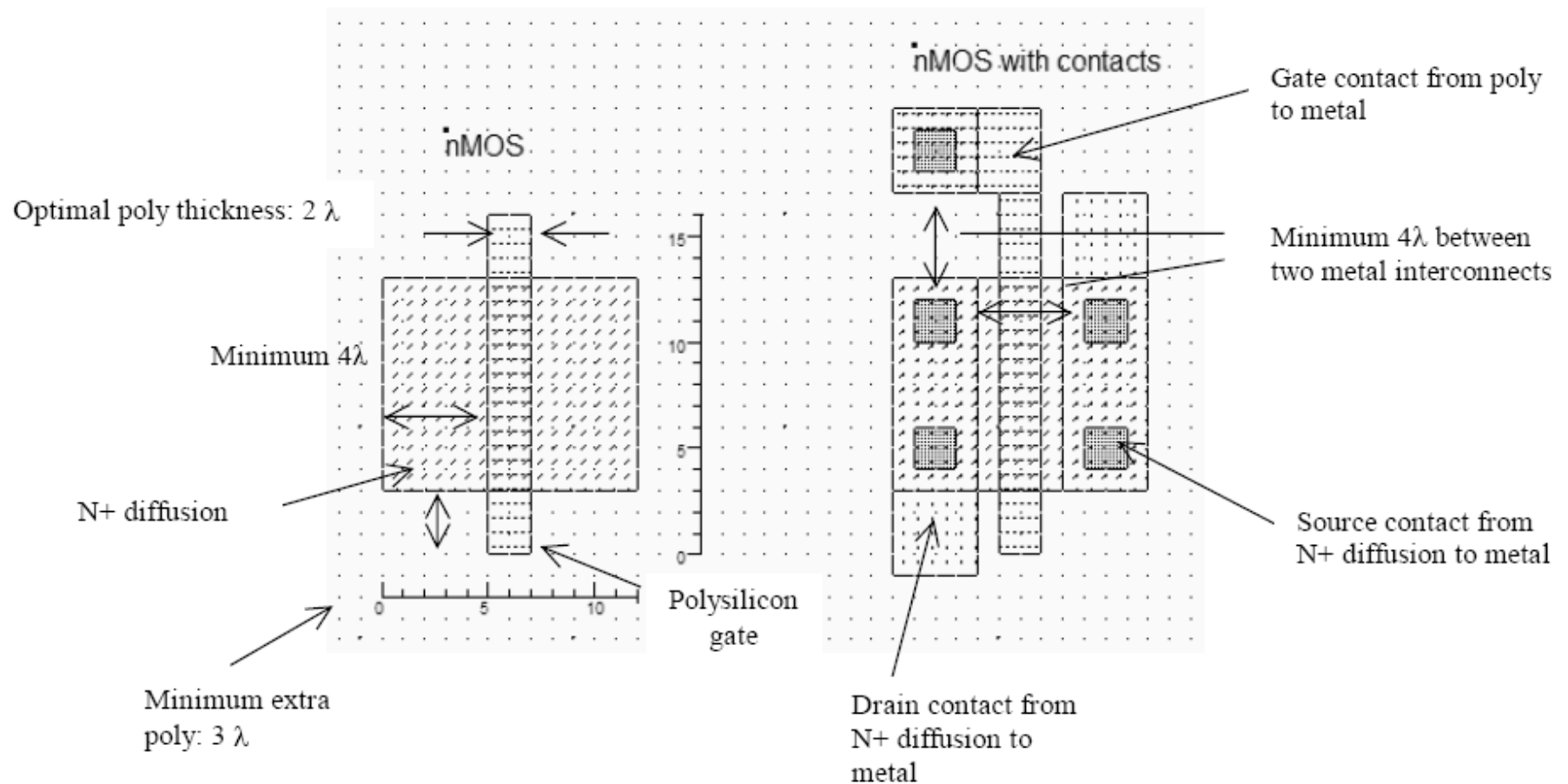


Figure 2-15: Vertical cross-section of an n-channel and p-channel MOS devices in 0.12µm technology

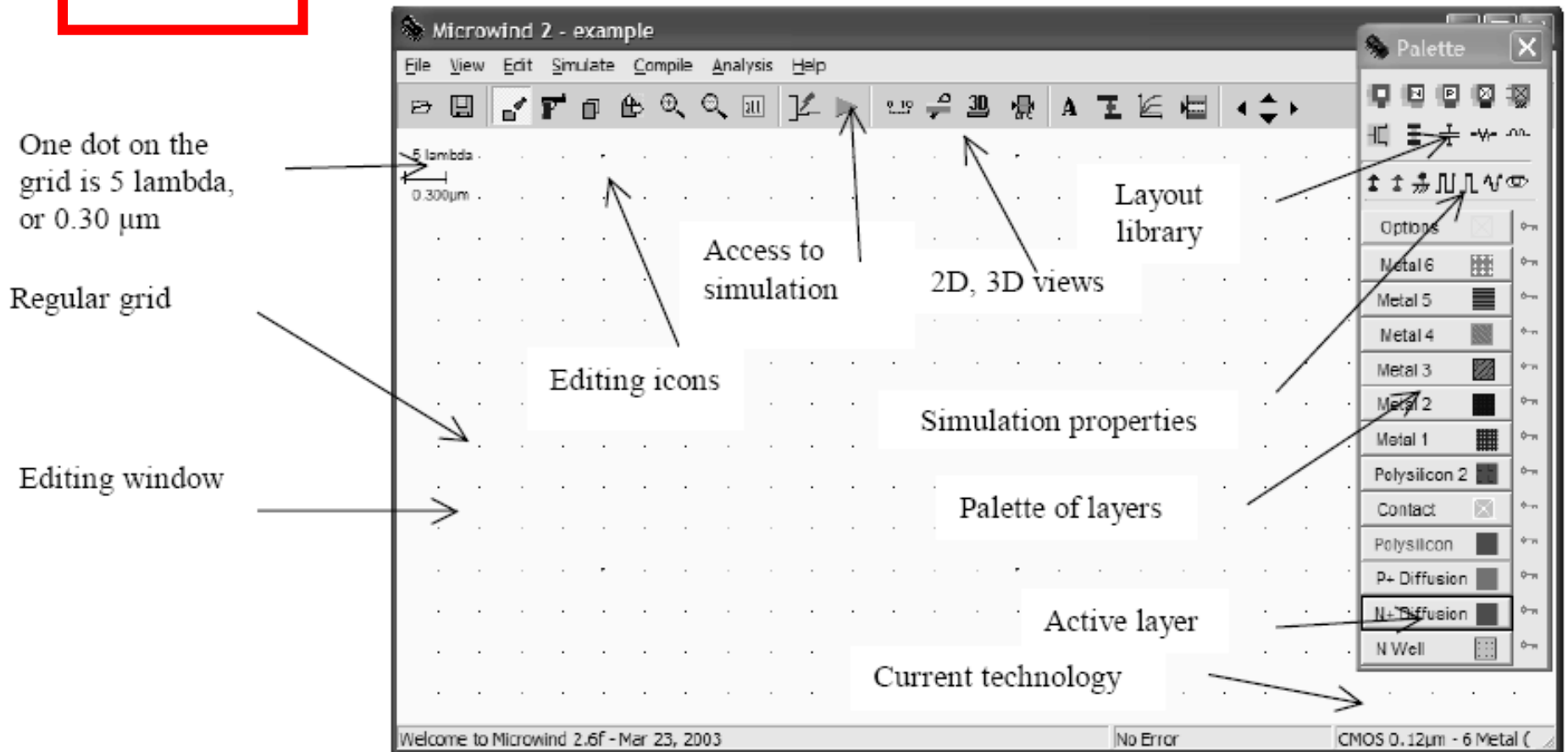
MOS transistor layout



microwind

$$\lambda = \frac{L_{\min}}{2}$$

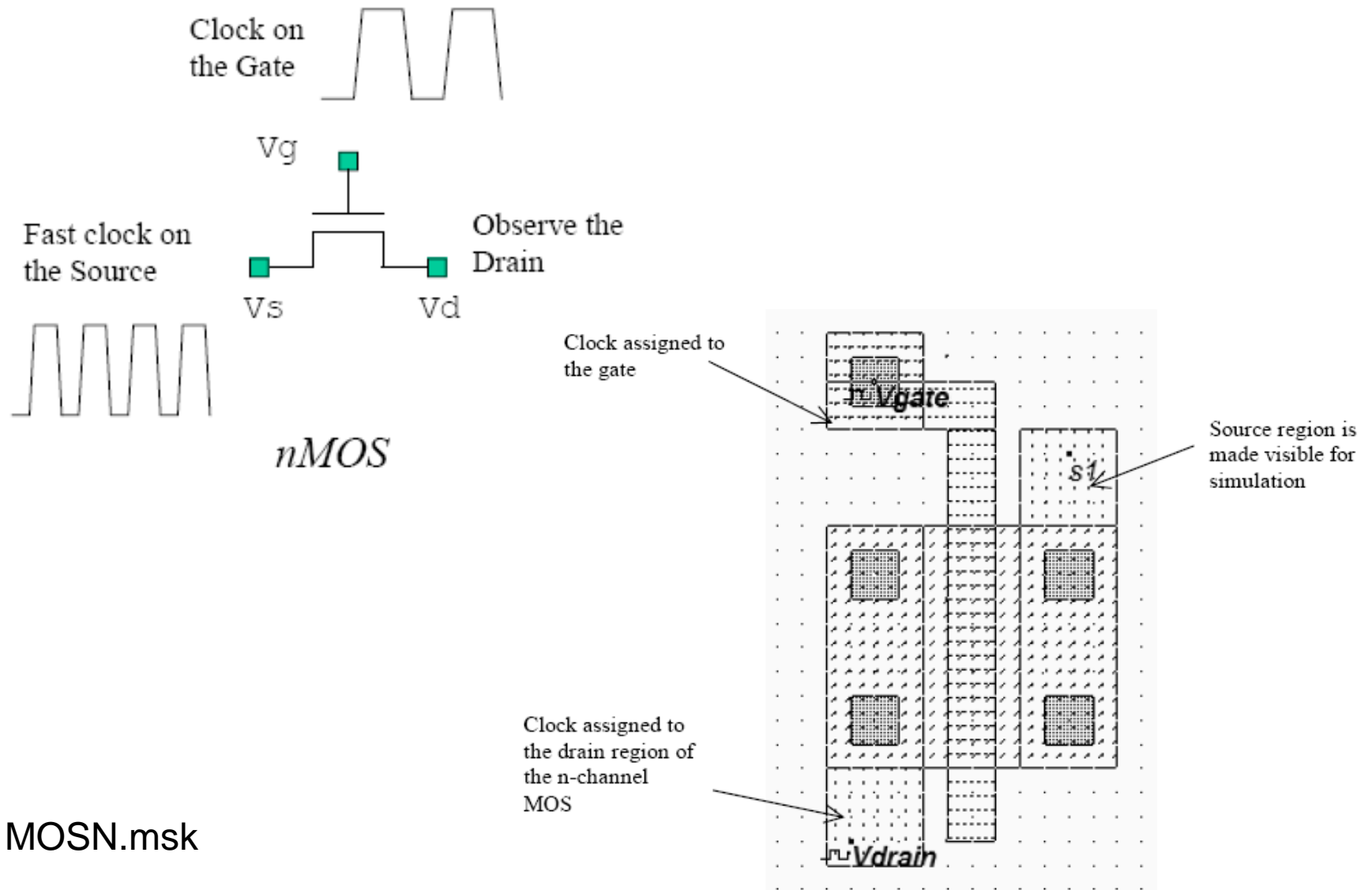
0.12 um CMOS process



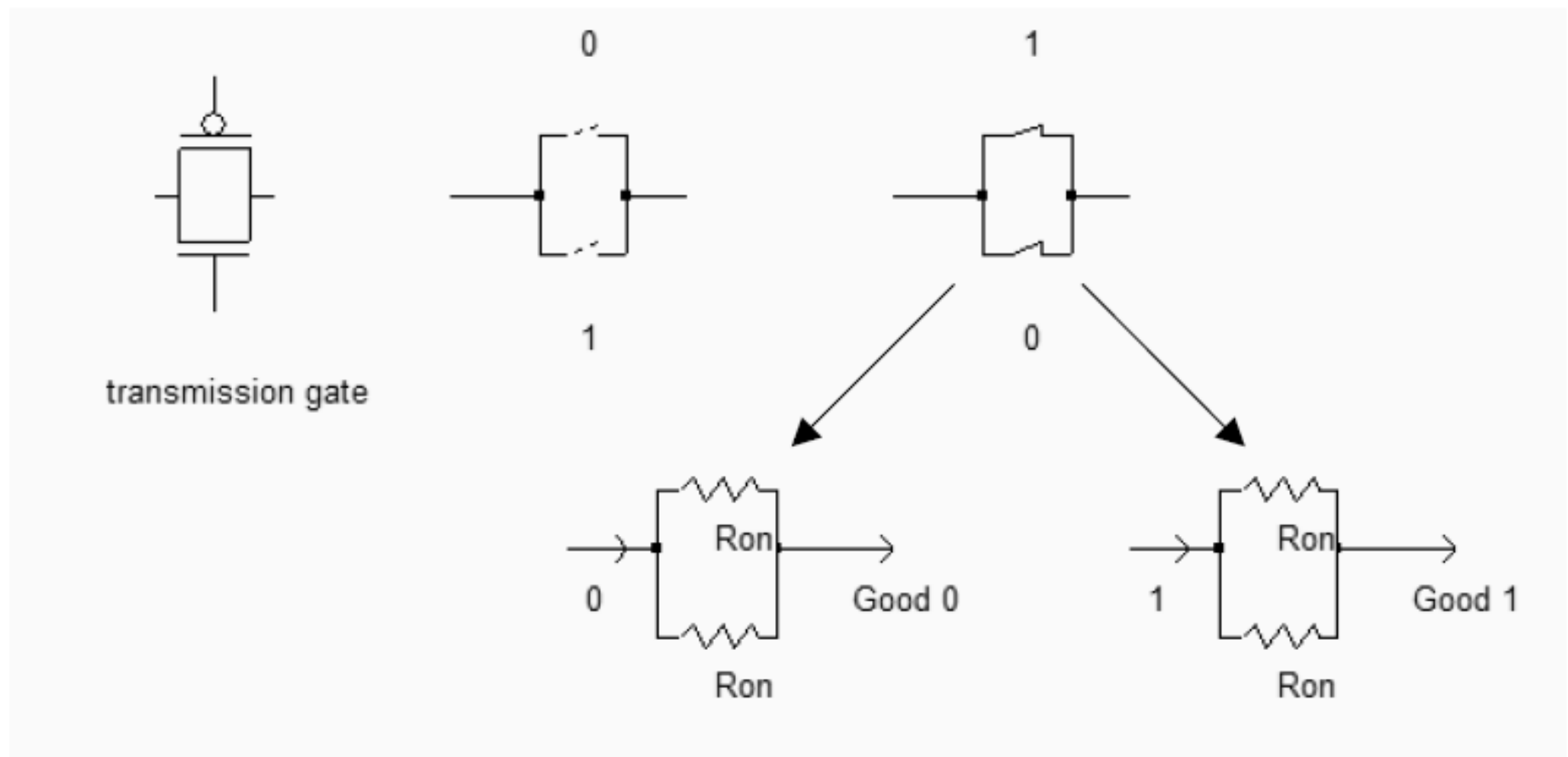
more notation

Layer name	Code	Description	Color in Microwind
Polysilicon	Poly	Gate of the n-channel and p-channel MOS devices	Red
N+ diffusion	Diffn	Delimits the active part of the n-channel device. Also used to polarize the N-well	Dark green
P+ diffusion	Diffn	Delimits the active part of the p-channel device. Also used to polarize the bulk	Maroon
Contact	Contact	Makes the connection between diffusions and metal for routing. The contact plug is fabricated by drilling a hole in the oxide and filling the hole with metal.	White cross
First level of metal	Metal1	Used to rout devices together, in order to create the logic or analog function	Blue
N well	Nwell	Low doped diffusion used to invert the doping of the substrate. All p-channel MOS are located within N well areas.	Dotted green

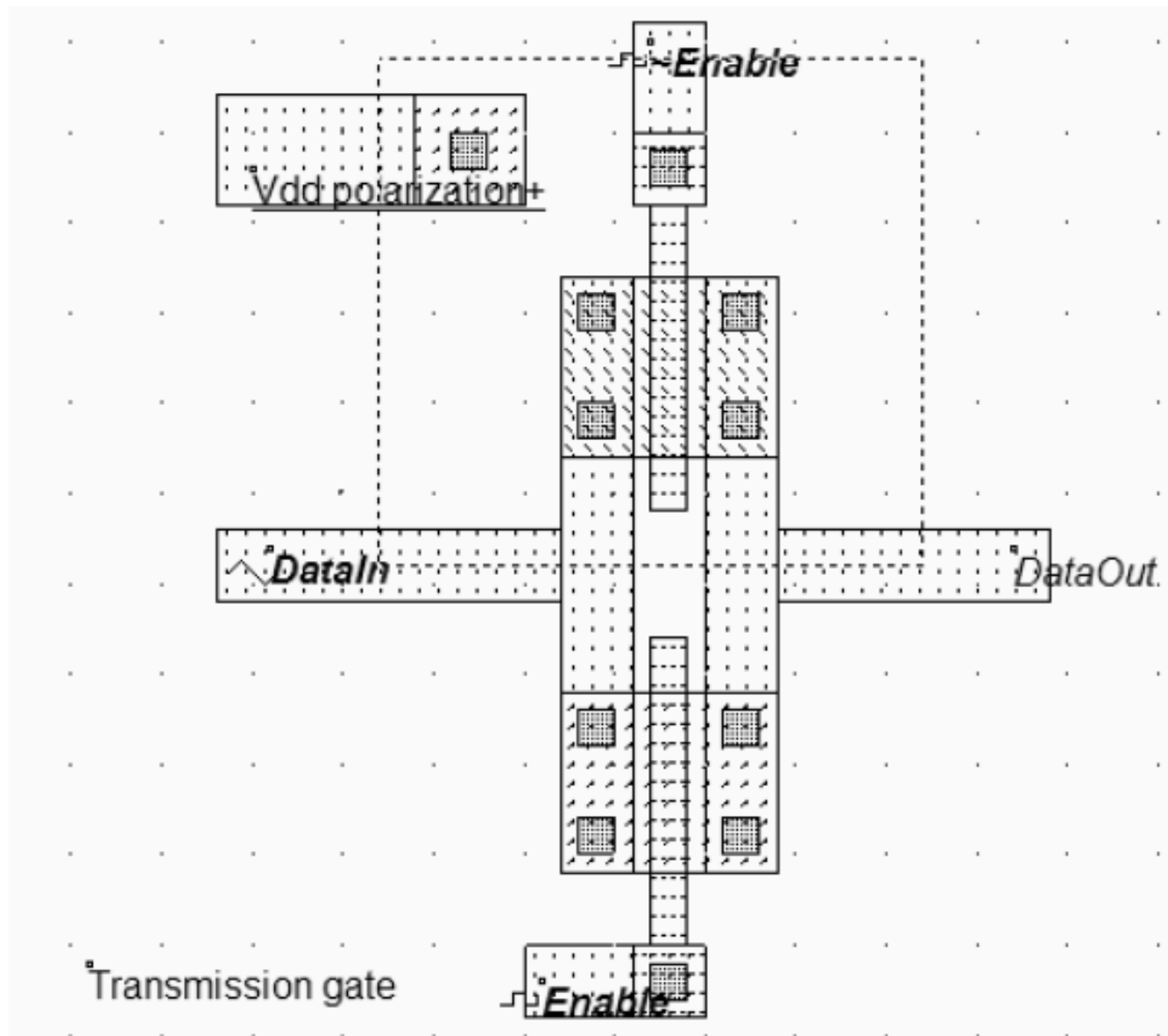
dynamic behavior: another level of abstraction



and the perfect switch!



simulation of the perfect switch



multiple contacts: why?

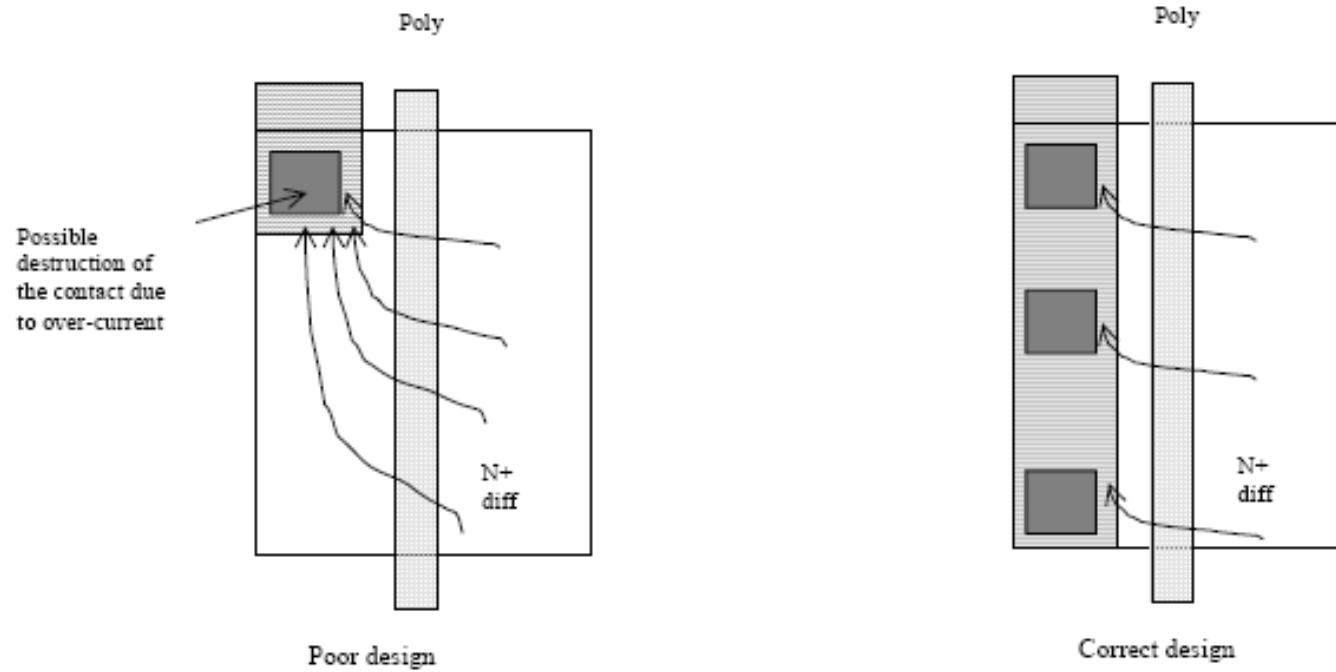


Fig.2-46. A strong current through a single contact could damage the metal structure.

multiple contacts

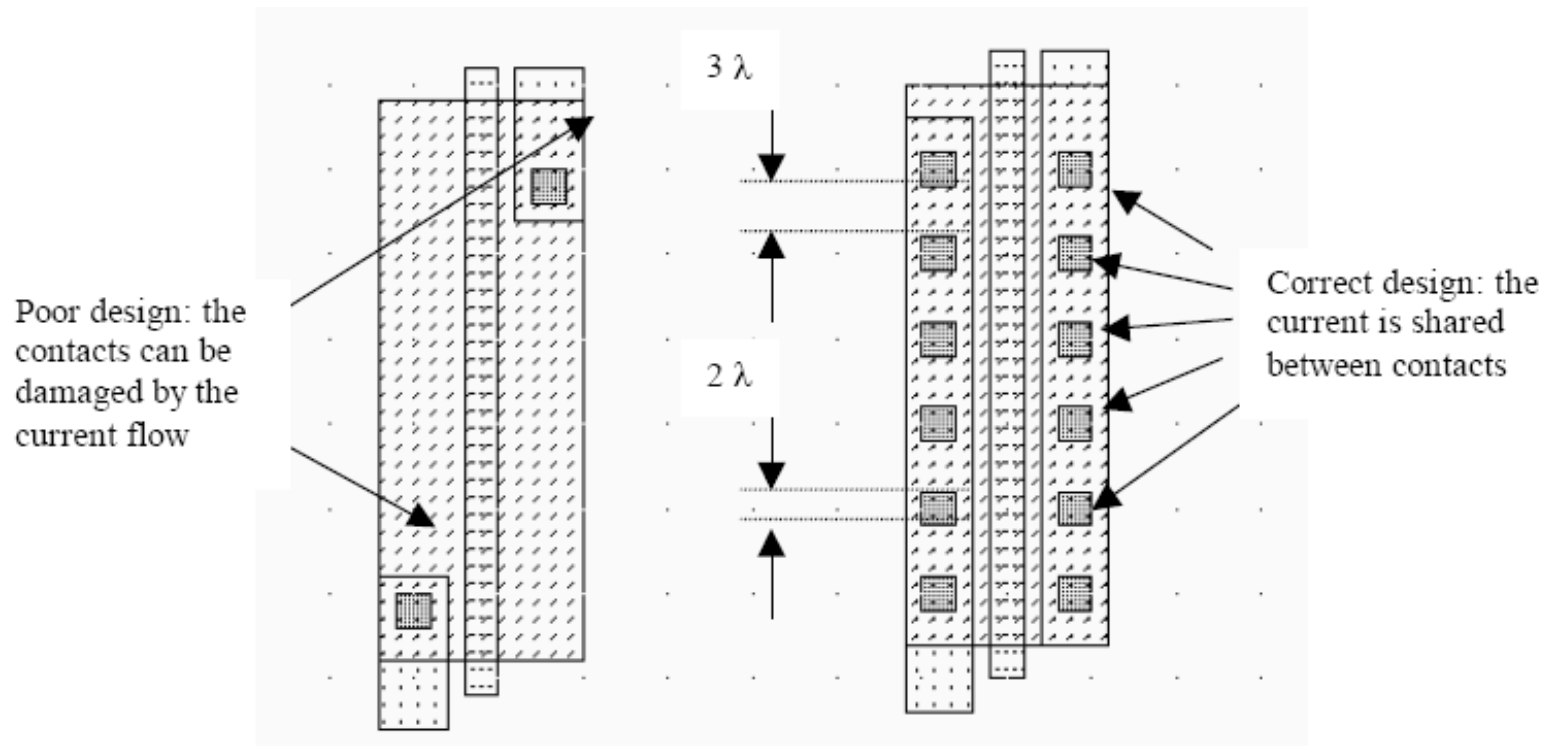


Fig.2-47. A single contact cannot handle more than 1mA. A series of contacts is preferred (MosLayout.MSK)

multiple contacts

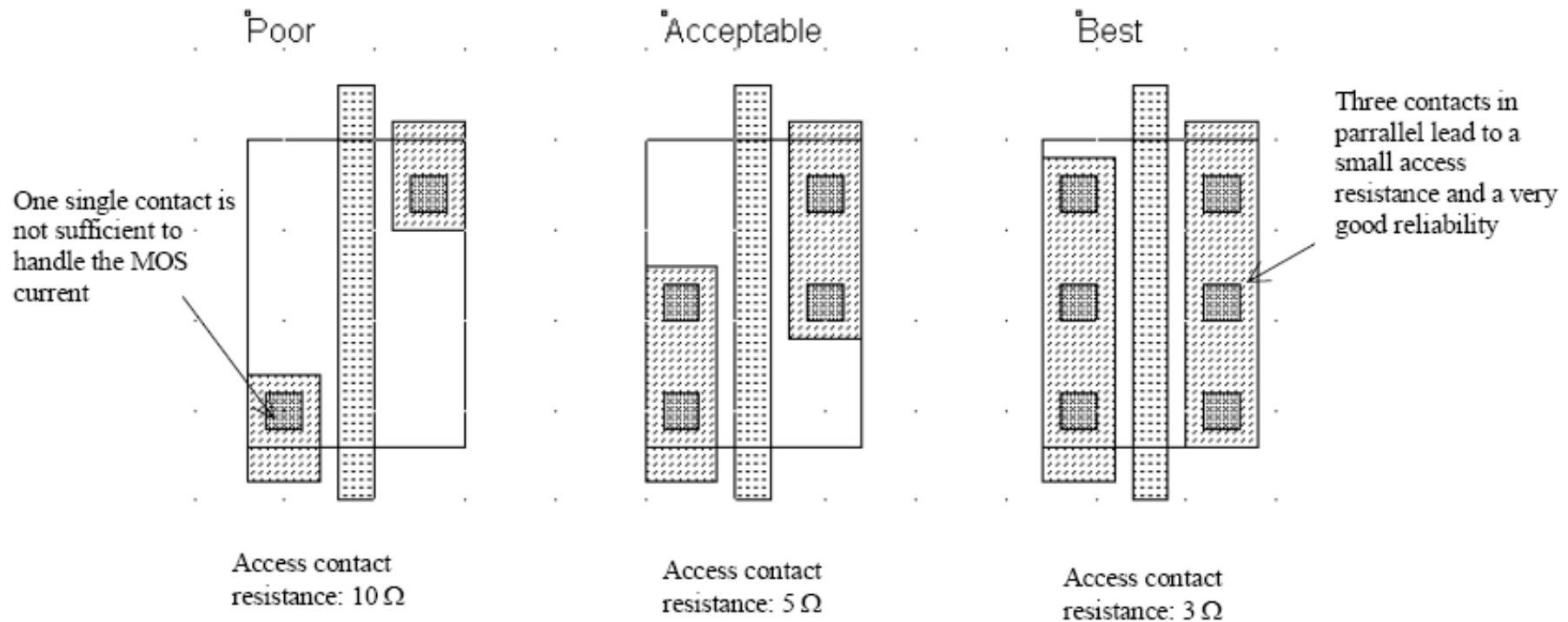
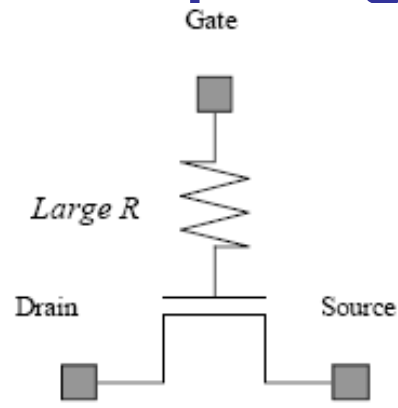
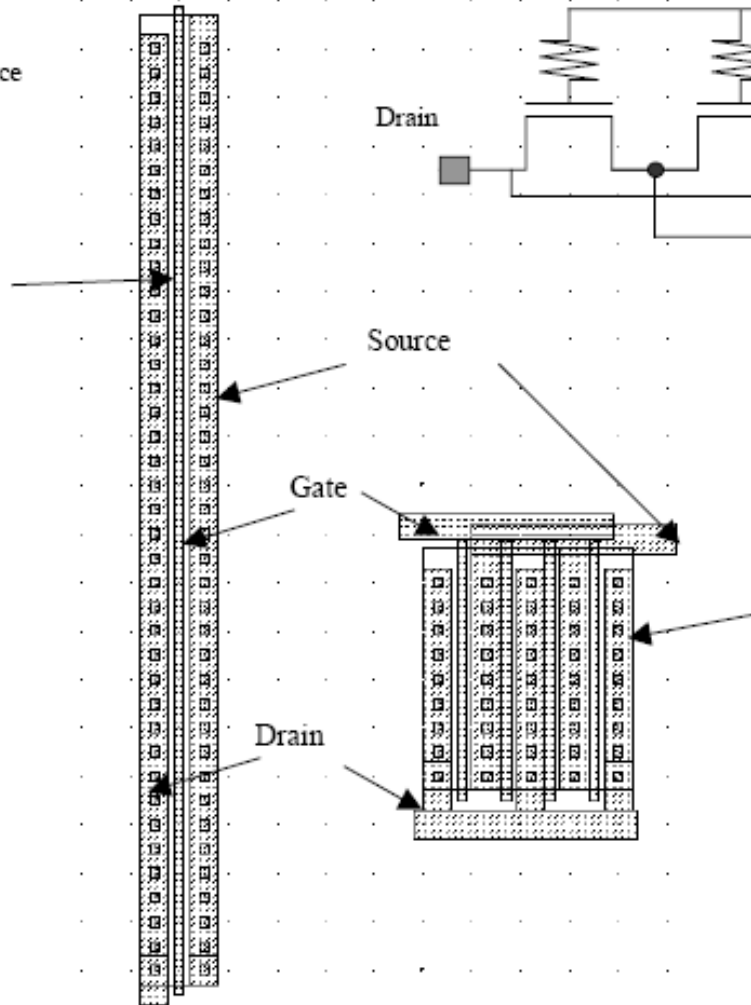
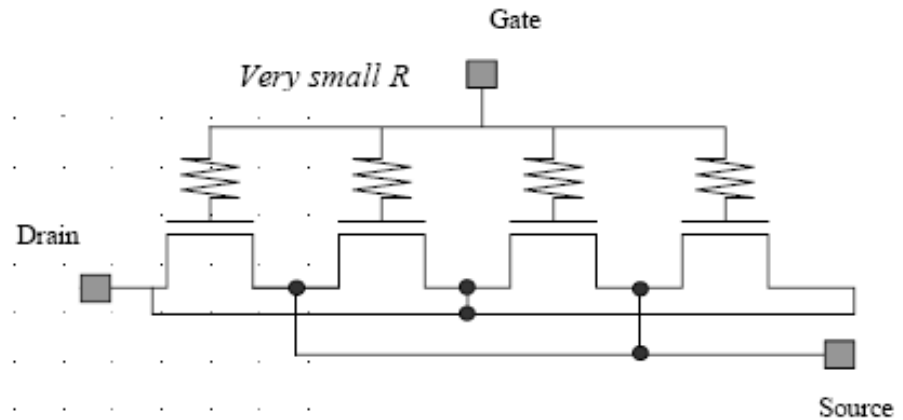


Fig.2-48. A series of contacts also reduced the serial access resistance(MosContacts.MSK)

multiple gates



Poor design : very tall structure and huge propagation delay within the gate



Correct design : regular structure, reduced propagation delay thanks to parrallel gates